PDCAT2005,Dalian, China

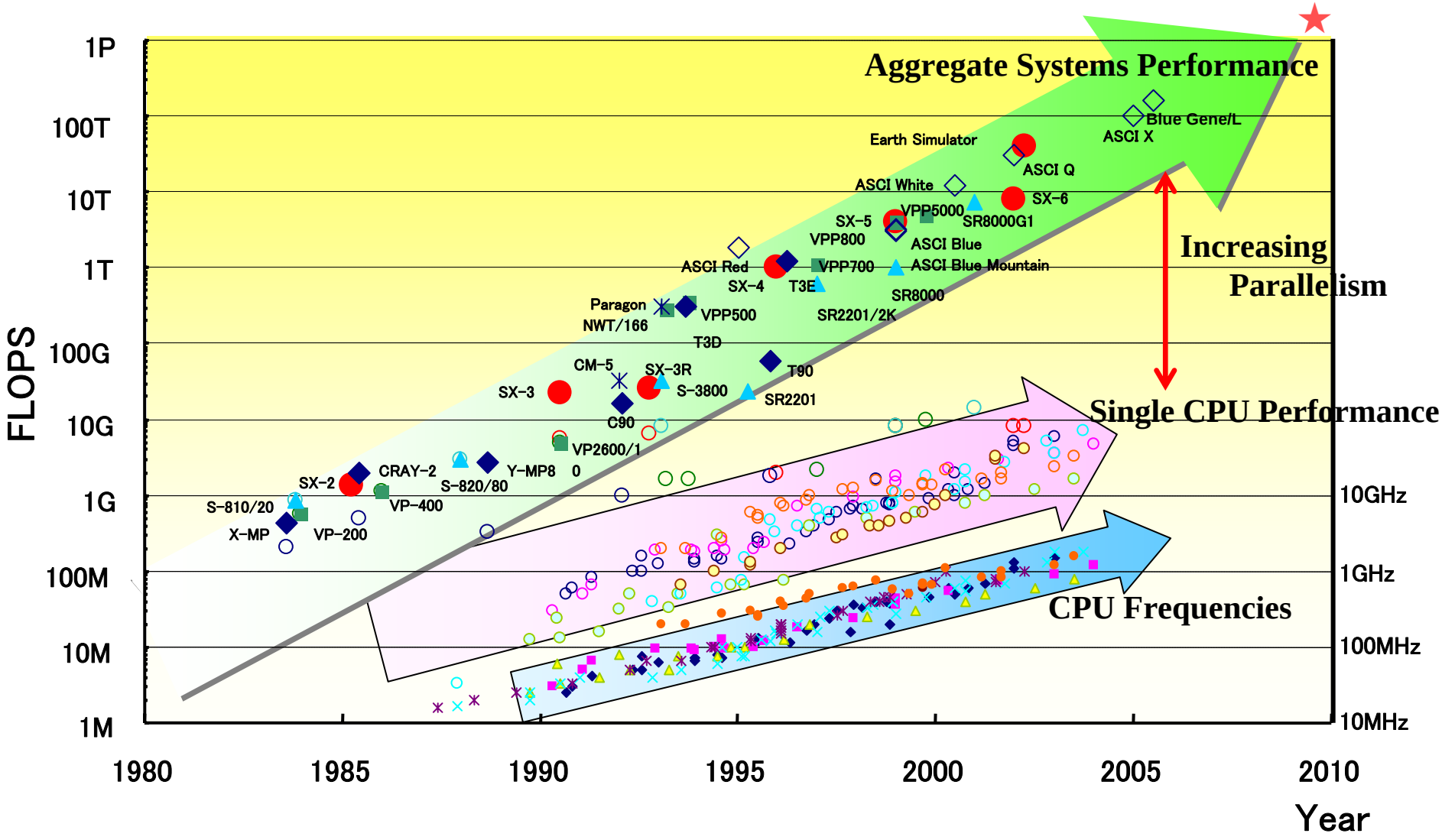
Future Technological Challenges for High Performance Computers

Dec.6, 2005

NEC

Tadashi Watanabe

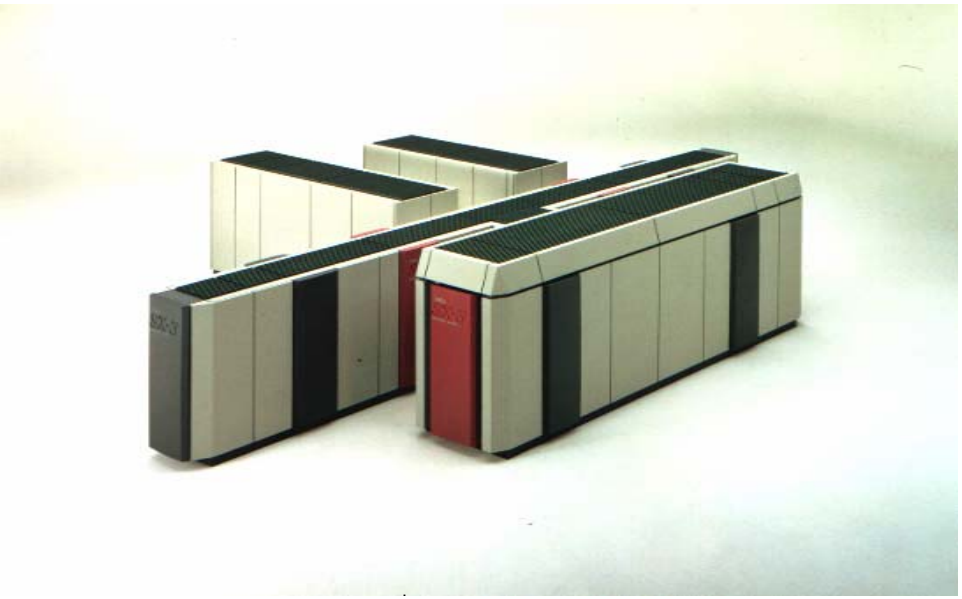
History of High Performance Computers



NEC

The Faster the Speed, the More the Parallel

The Largest configuration in SX-3



22GFlops/4Cpu

1990

10Years

The Earth Simulator

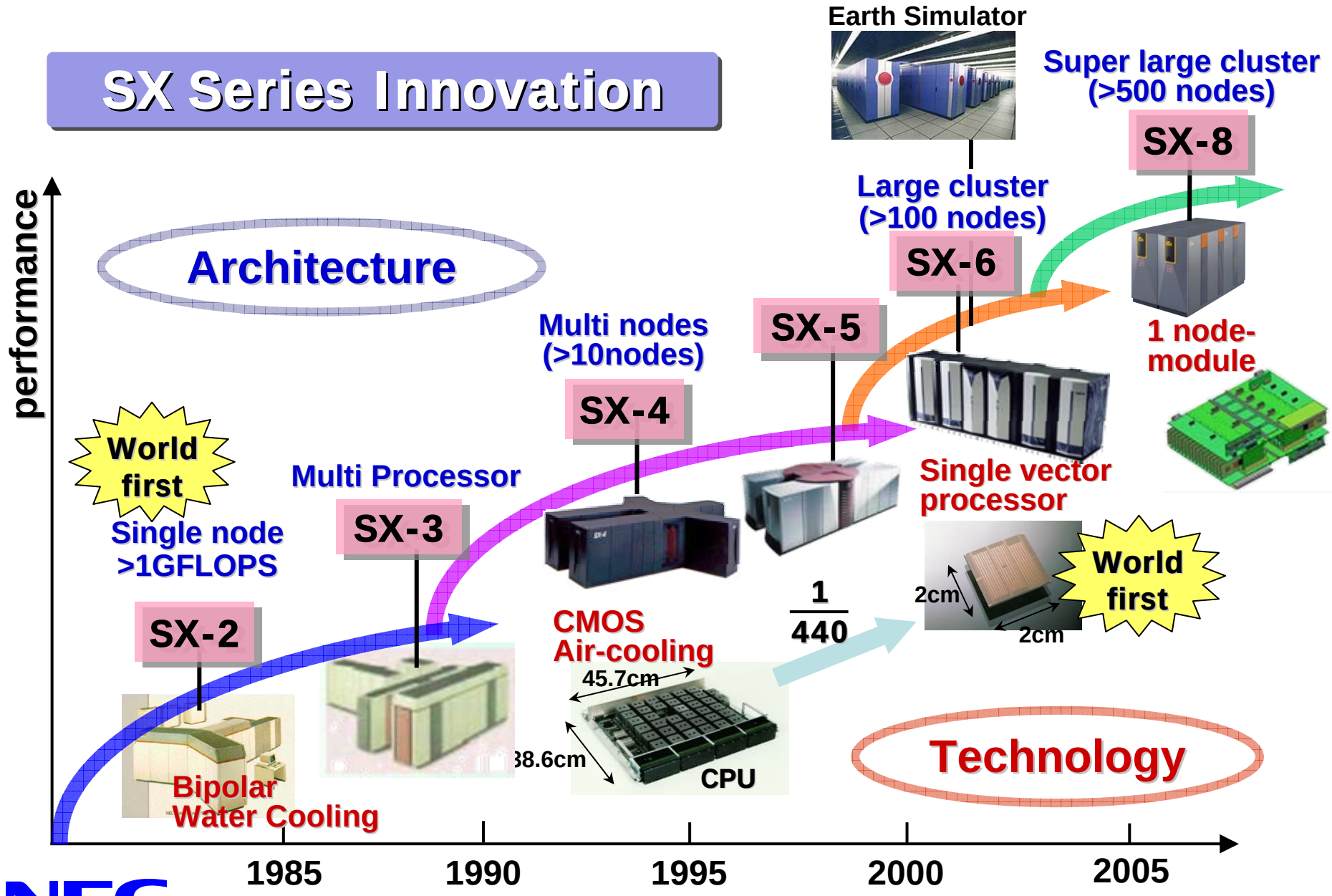
40TFlops/5120Cpu

2002

NEC

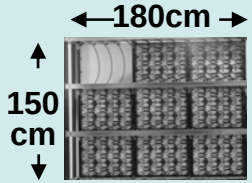
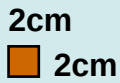
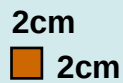
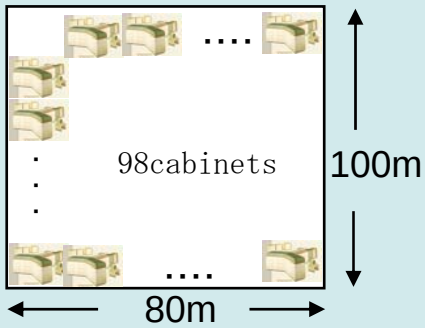
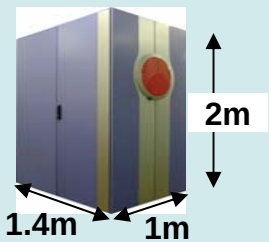
History of SX Series

SX Series Innovation



NEC

Evolution of SX Series for 20 years

	'83(SX-2)	'02 (EarthSimulator)	'04 (SX-8)	(SX-8/SX-2)
CPU Performance	1.3GFLOPS	8GFLOPS	16GFLOPS	×12
System Performance	1.3GFLOPS	40TFLOPS	65TFLOPS	×50,000
# of CPUs	1	5,120	4,096	×4,096
Total Memory Capacity	256MBytes	10TBytes	64TBytes	$\times 2.6 \times 10^5$
CPU Size				×1/6,750
#of chips per CPU	2,250chips	1chip	1chip	×1/2,250
System Size				×1/9,400

NEC

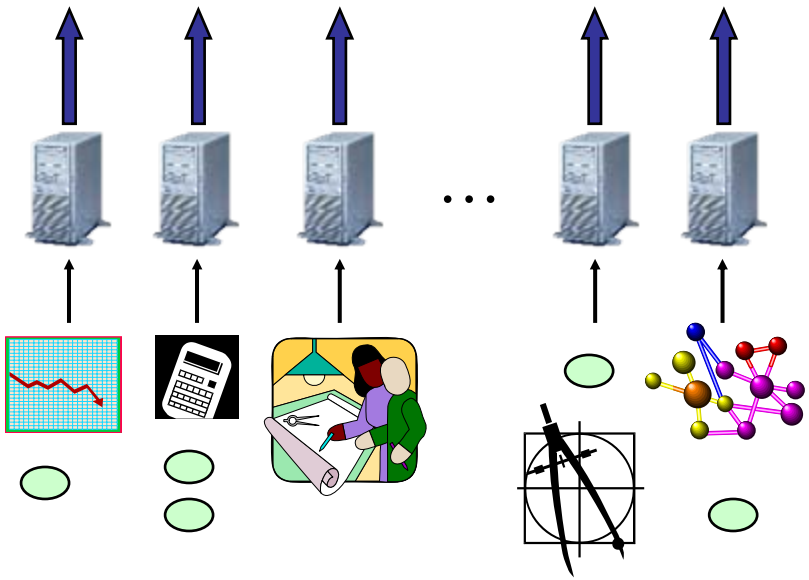
Will this technological evolution continue?

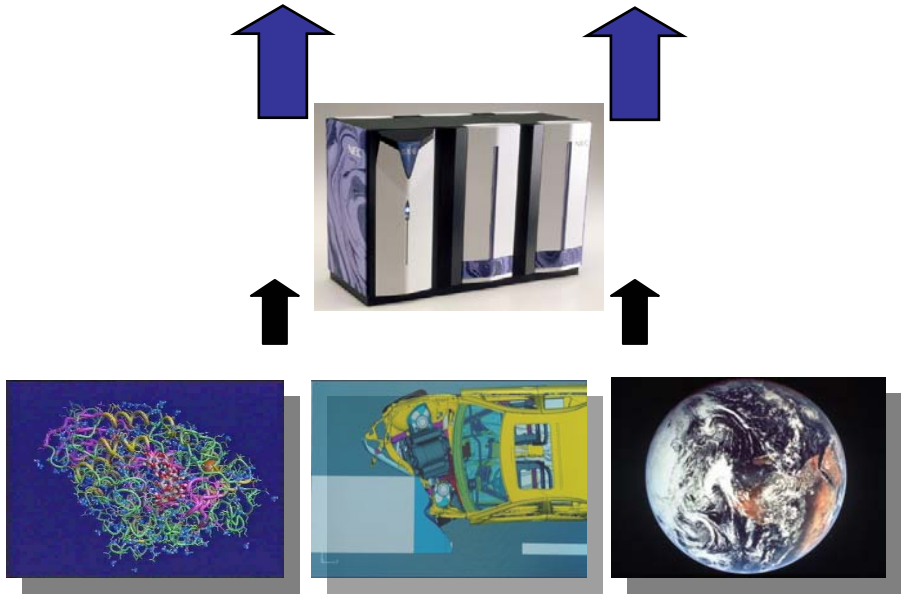
Are there any problems or difficulties to overcome?

If so, what are they?

NEC

Capacity Computing and Capability Computing





PC Cluster / Blade Server

Vector / SX

Capacity Computing

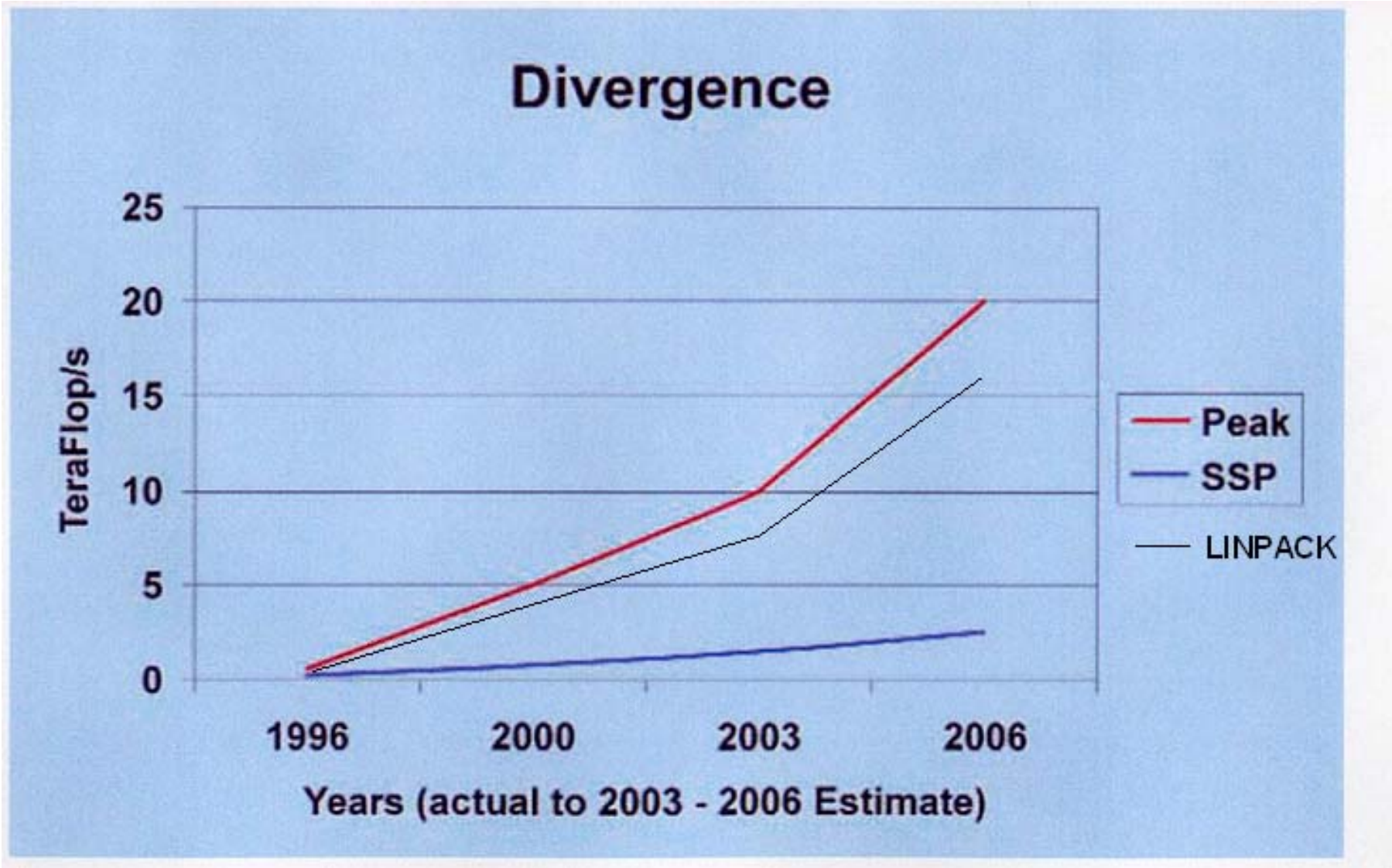
- Goals: Workload and Throughput Many Jobs per time
- Many Small Problems
- Parallel or Cluster Machine based on Microprocessor

Capability Computing

- Goals: High Speed Execution of Single Job
- Large and Critical Problem – Grand Challenge
- Powerful Processor and Highbandwidth Network

NEC

Divergence Problem

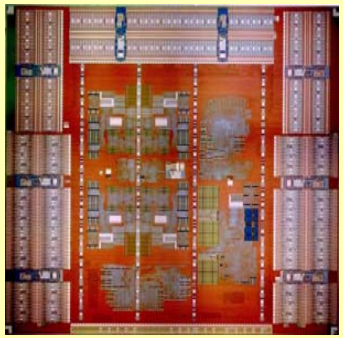


（Report by HECRTF）

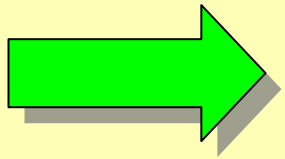
NEC

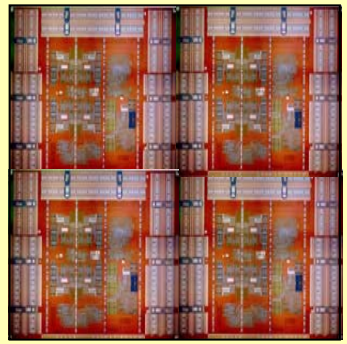
Multi Core Technology for Capacity Computing

Device Technology



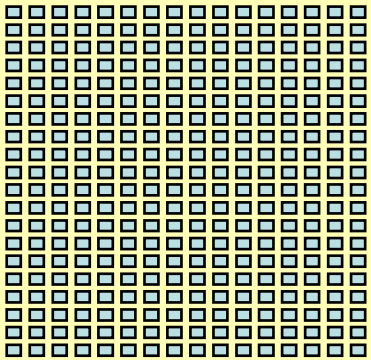
Single Core

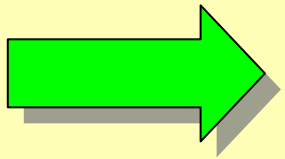


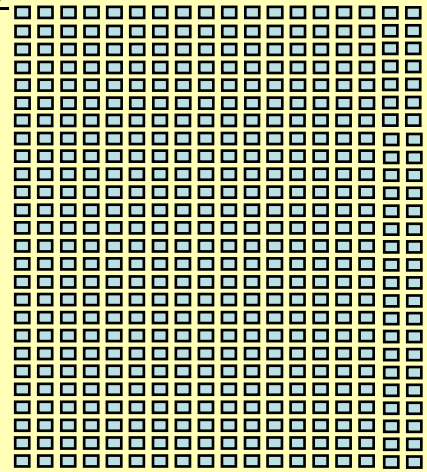


Multi Core

System Technology
(Parallelism)





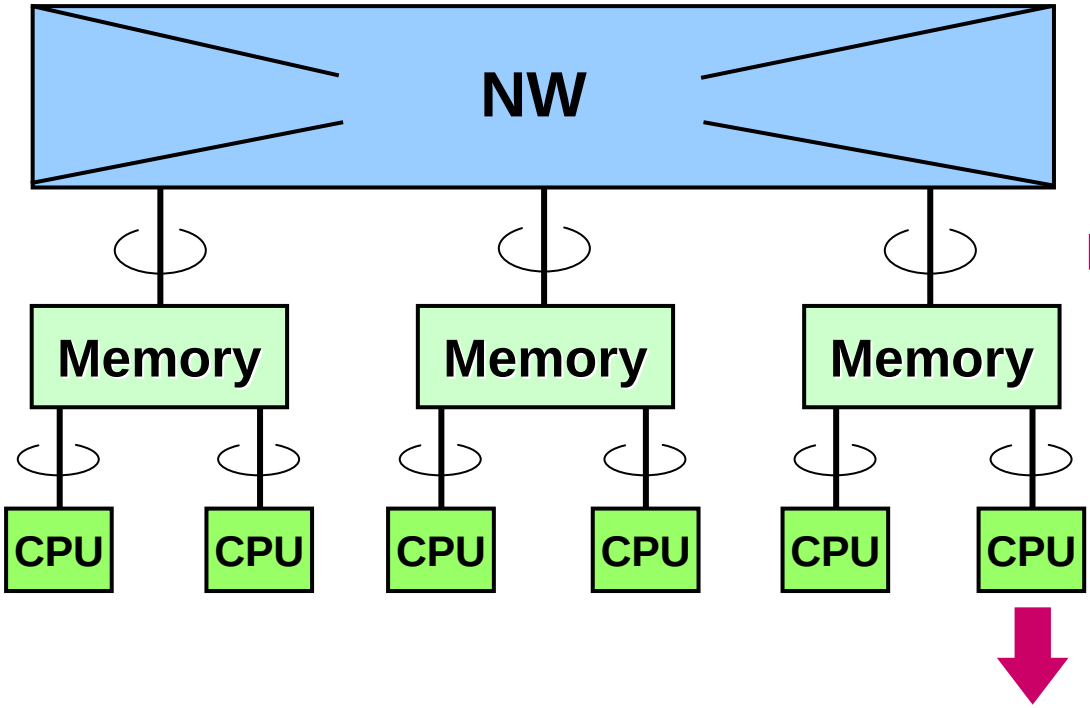


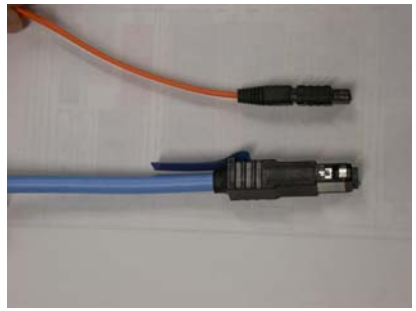
More Parallel

Speed incease by more parallelism is not a solution to divergence problem

NEC

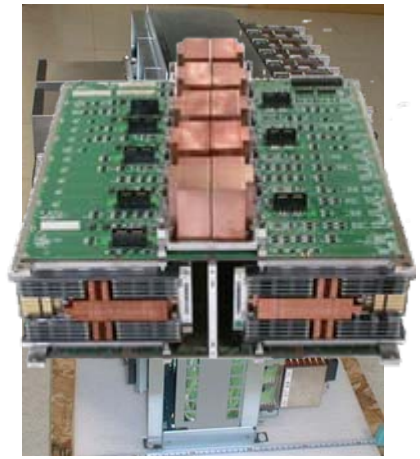
Highly Efficient Capability Computing

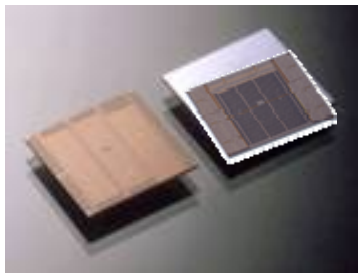




- Low Latency
- High Throughput

High Bandwidth Interface





Powerful CPU

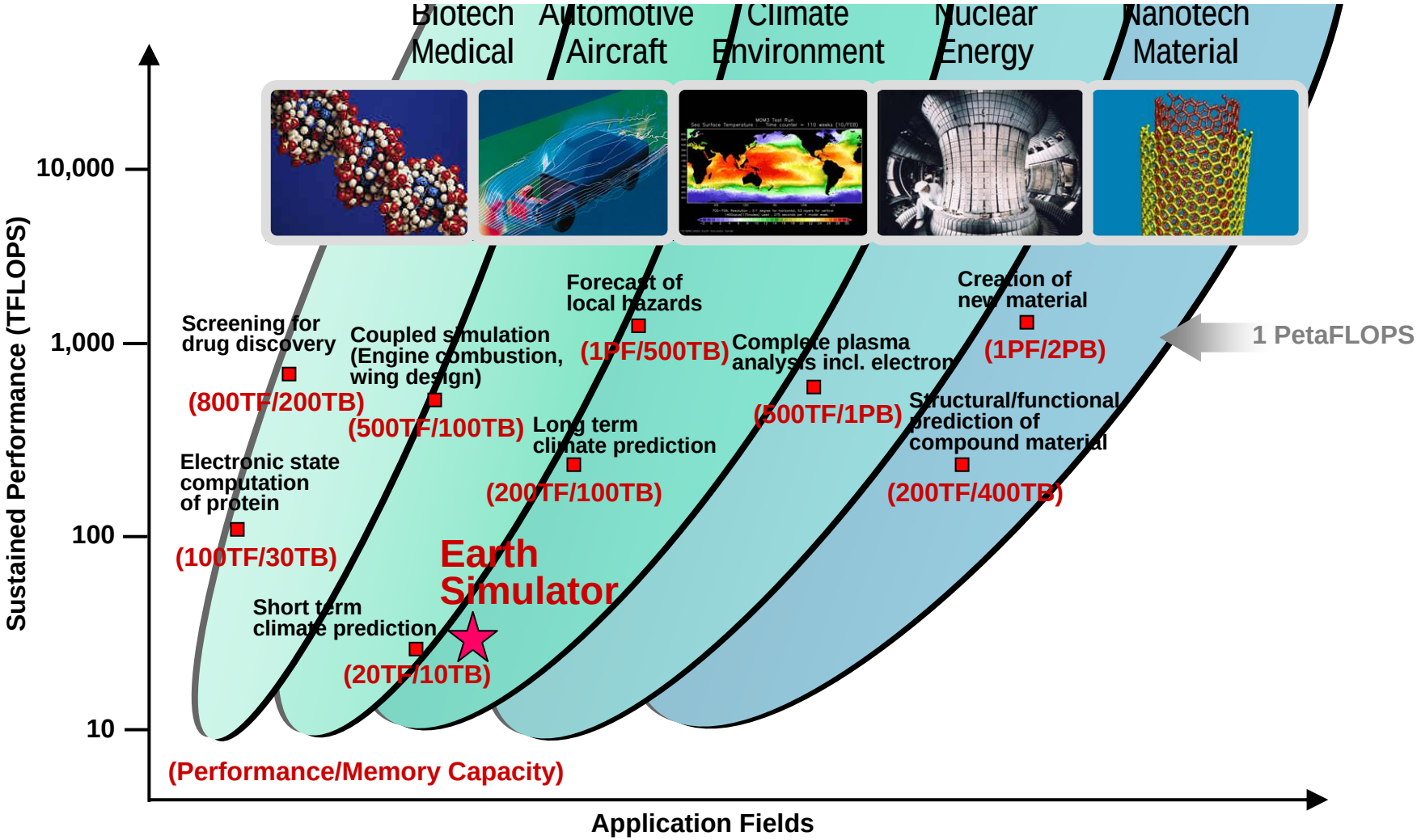
NEC

Future Technologies for Capability Computing

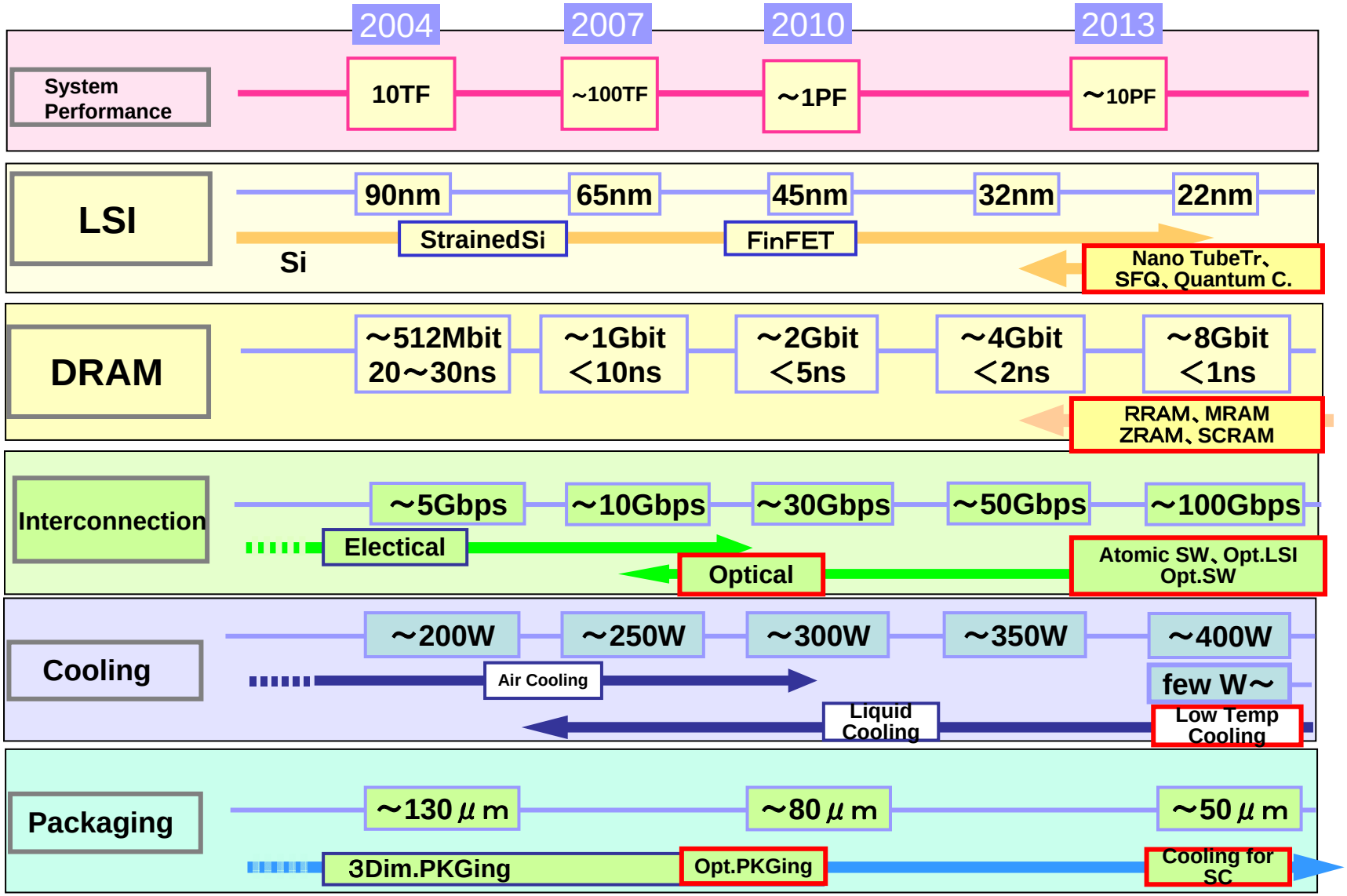
NEC

The Future of PetaFLOPS Computing

Applications and Required Performance

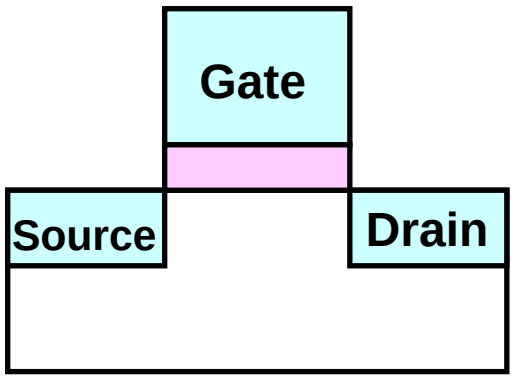


Technology Road Map

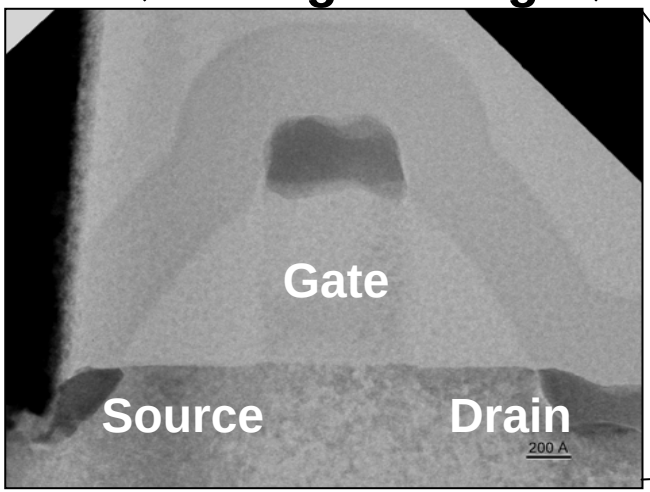


NEC

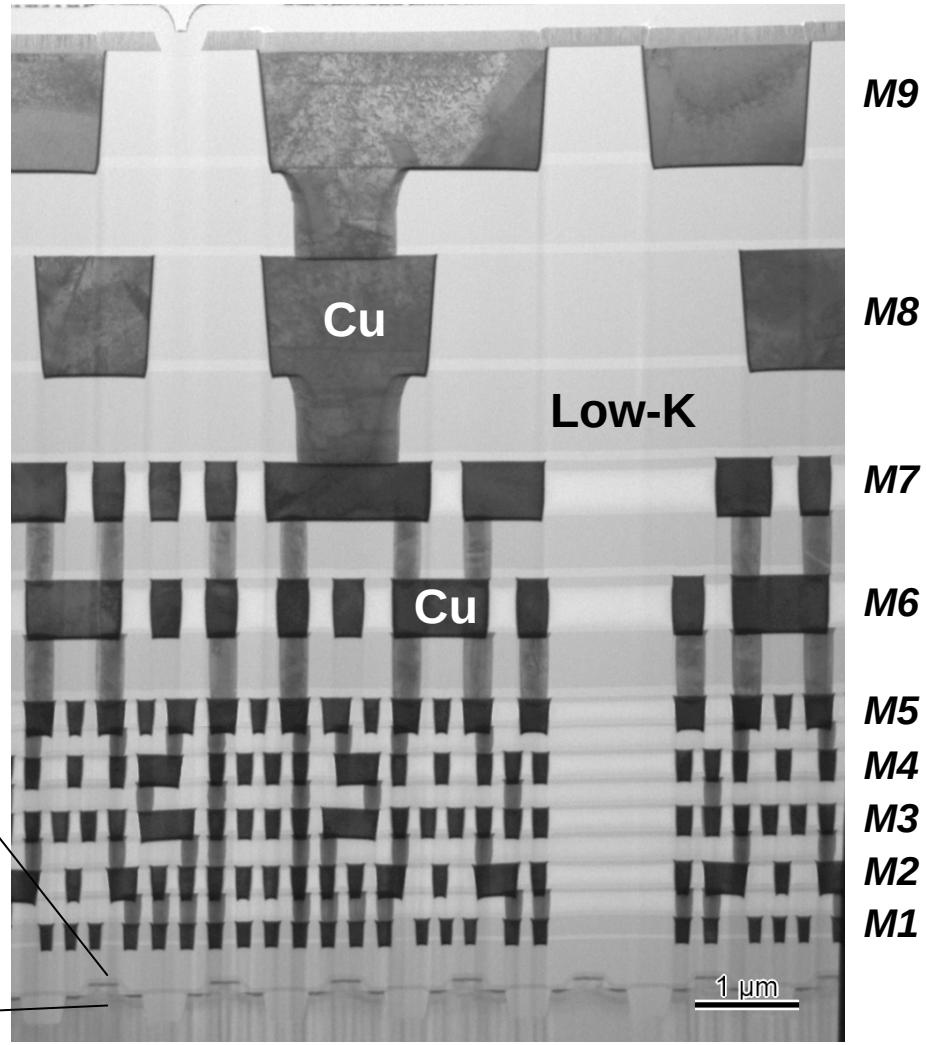
Structure of LSI: UX6（CB90H）



Tr（60nm gate length）



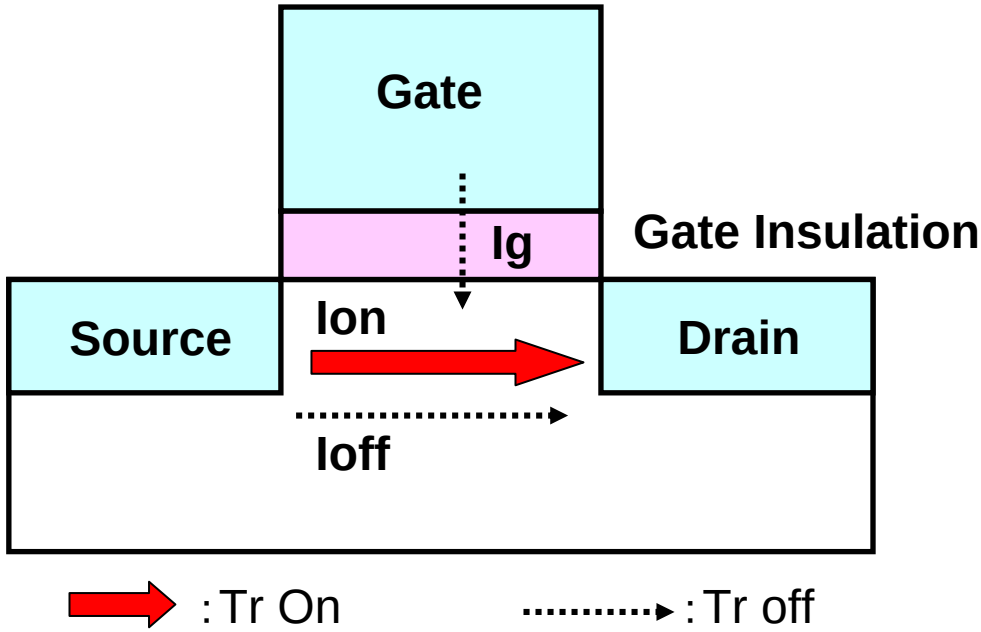
9 layers Cu/Lowk(2.9) wiring



写真提供： NECエレクトロニクス（株）

NEC

Structure of Tr

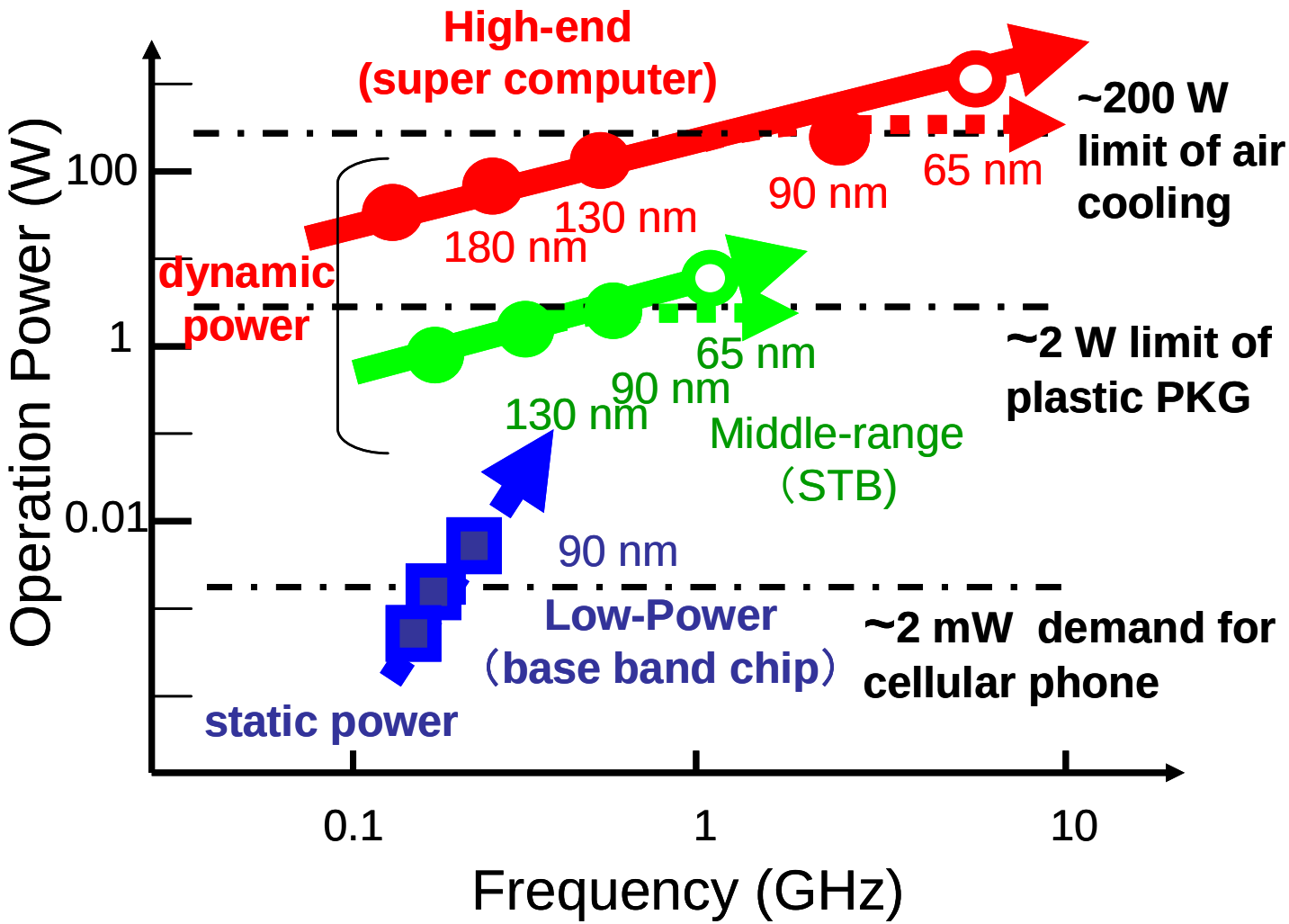


$$\text{Power} = \frac{f \cdot Ci \cdot v^2}{\text{Op} \cdot \text{Power(wiring)}} + \frac{f \cdot Ct \cdot v^2}{\text{Op} \cdot \text{Power(Tr)}} + \frac{(Ioff+Ig) \cdot v}{\text{Std-by Power}}$$

NEC

Power dissipation trend

Problems of conventional scaling appear in the power dissipation



NEC

Power Dissipation and Cooling

Power consumption (W)

10k

1k

100

10

1

1995

2000

2005

2010

Year

0.35um

0.25um

0.18um

0.13um

0.09um

2000 l/min

250 l/min

100 l/min

25 l/min

15 m/s

6 m/s

3 m/s

0 m/s

Liquid cooling

Forced-conv. air cooling

Natural-convection air cooling

NEC

Technologies for Power Scaling

■ Operating Power

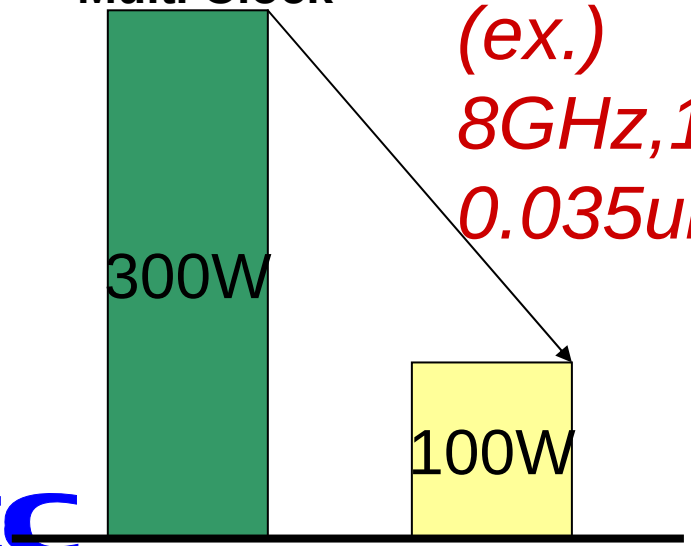
1) Device・Process
- ・Low-k Material
- ・Strained Si
- ・SOI

2) Circuit・Architecture
- ・Skew Design
- ・Self Clocking
- ・Clock Gating
- ・Multi Clock

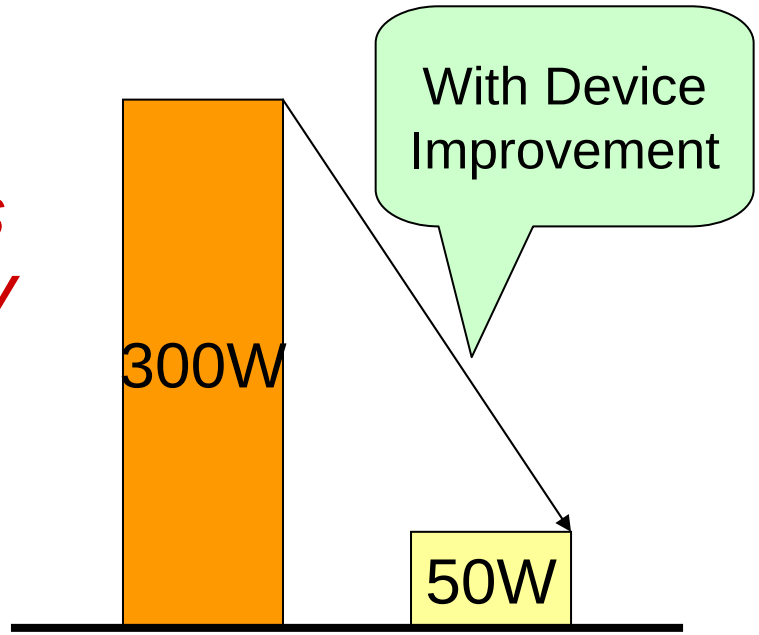
■ Stand-by Power

1) Device Process
- ・Multi Vt
- ・High-k Material

2) Circuit・Architecture
- ・Multiple Power
- ・Bias Control



(ex.)
8GHz,16cores
0.035um, 0.7V



NEC

New Technologies

NEC

Low Temperature CMOS

■ Advantages of Low Temperature

・Tr

⇒ Reduced Ioff exponentially

⇒ Higher Carrier Mobility（Faster Speed）

・Wiring

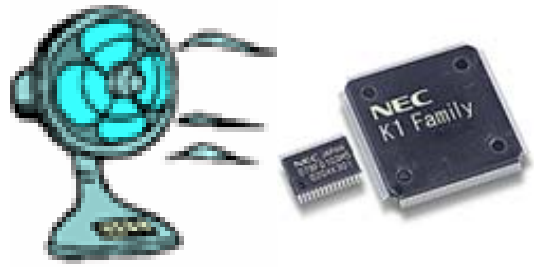
⇒ Reduction of Resistance

■ Required Technologies

・Highly Efficient Cooling

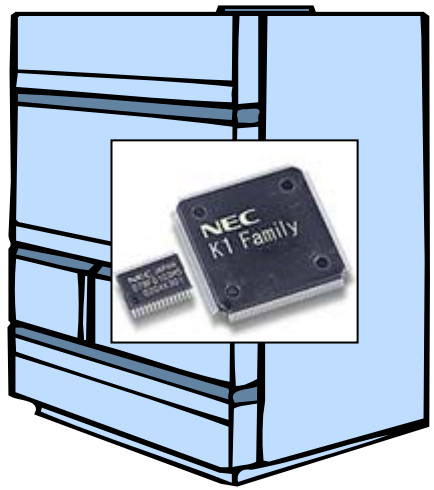
・Packaging for Low Temperature CMOS

（Board and Chip）



Current： 65℃

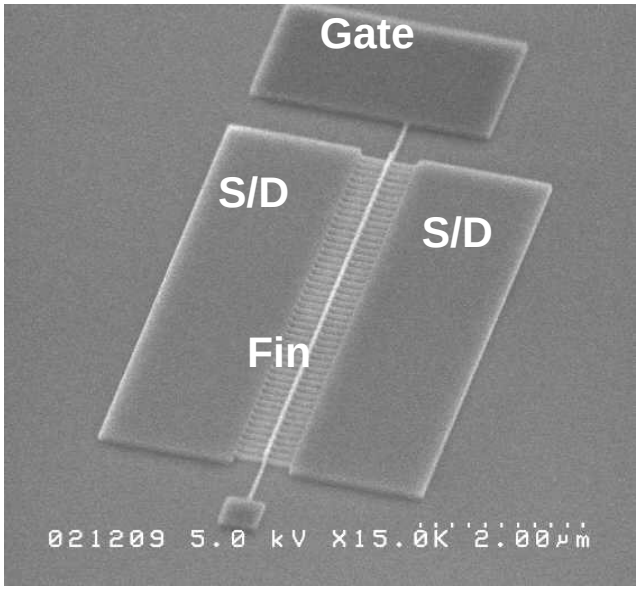
Future～ 0℃ ??

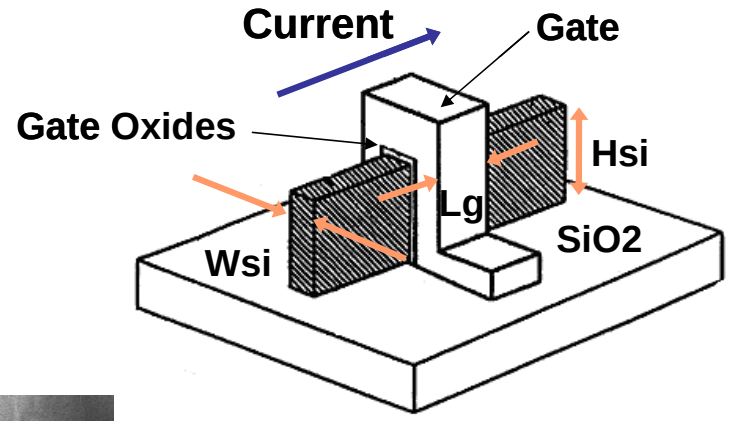


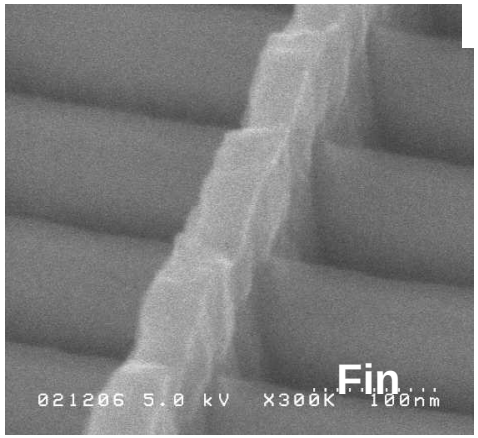
NEC

FinFET

- FinFET is one of 3D device structure.
- Good channel controllability, because of DG structure.
- New technologies are required to fabricate FinFETs.







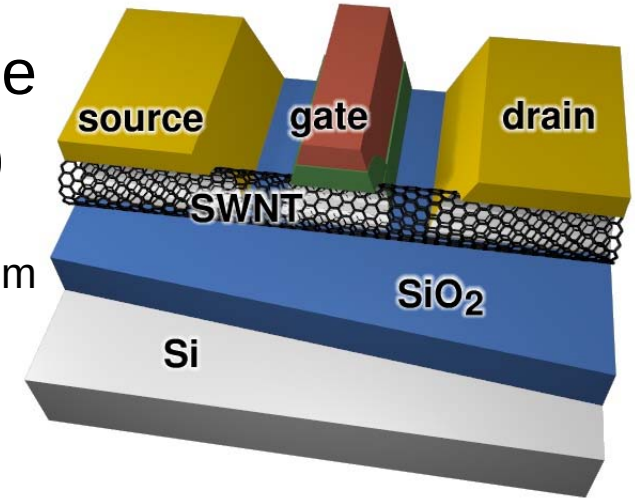
NEC

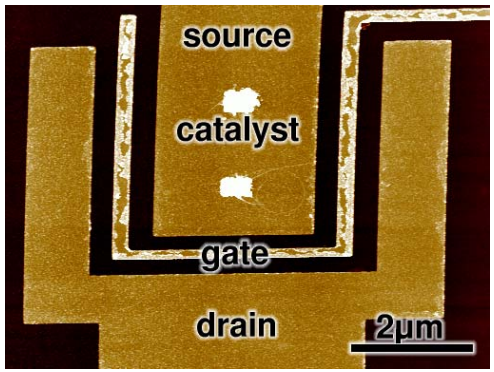
Carbon-Nanotube Field-Effect Transistors

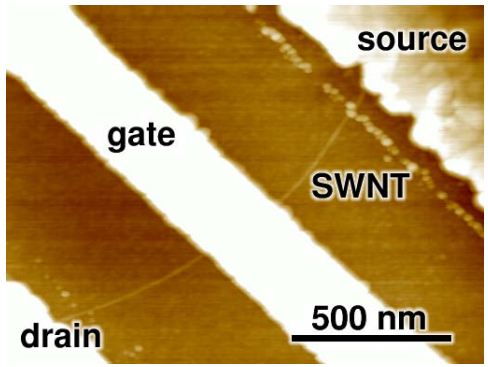
- Possible application: low-cost, low-power LSI, rf drivers
- Position-controllable on-wafer growth (catalyst CVD)
- Extremely high transconductance:

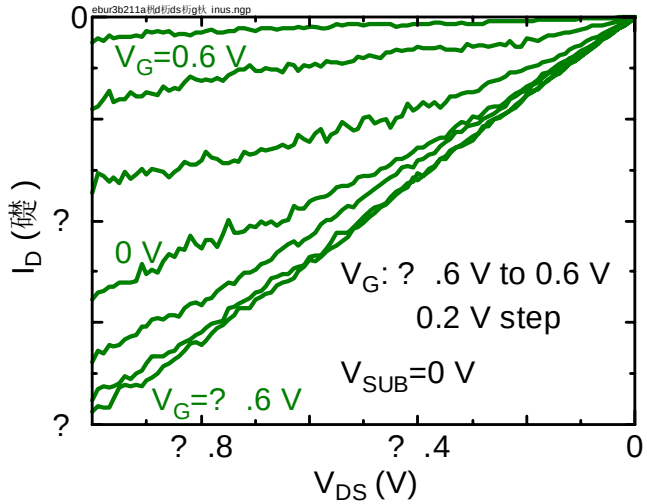
g_m=8.7 μS/tube
(5800 μS/μm)

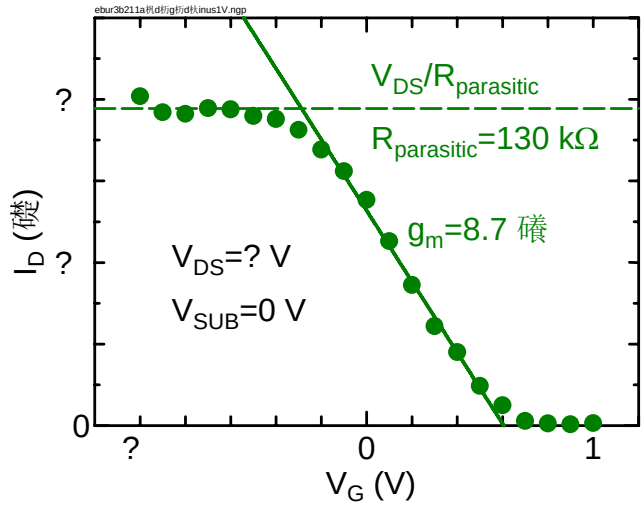
Si nFET: 1000~1200 μS/μm
pFET: 400~600 μS/μm





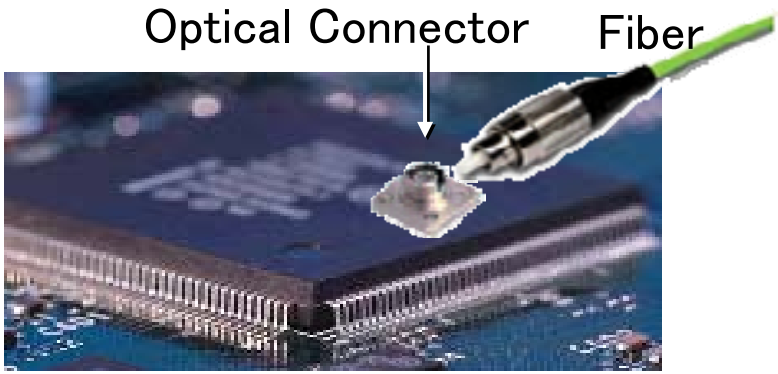


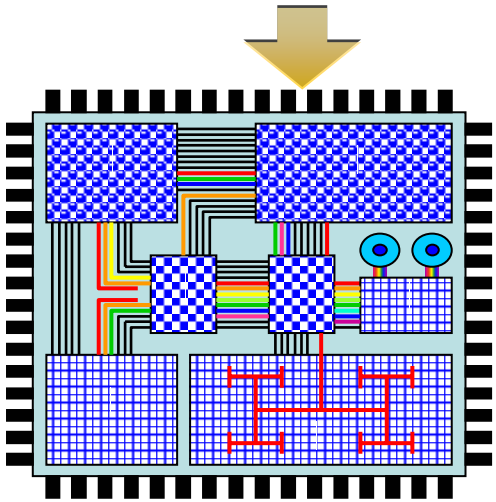




NEC

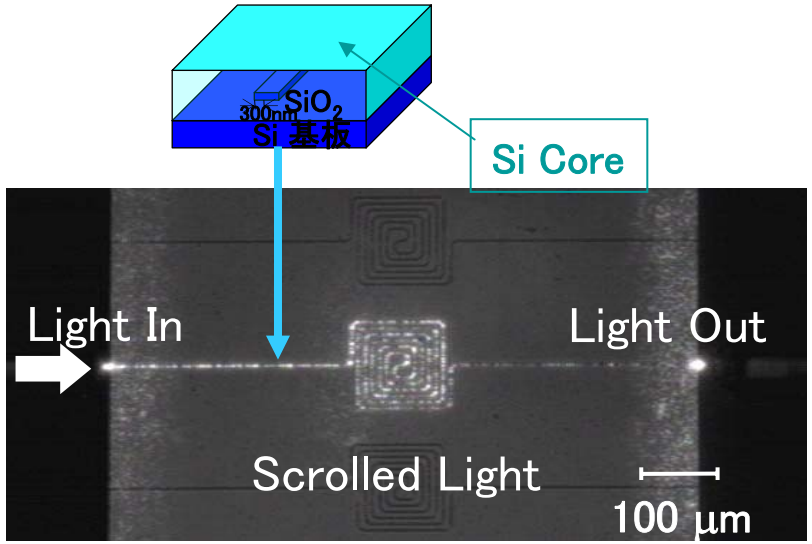
Si Nano Photonics（Optical Interconnections）





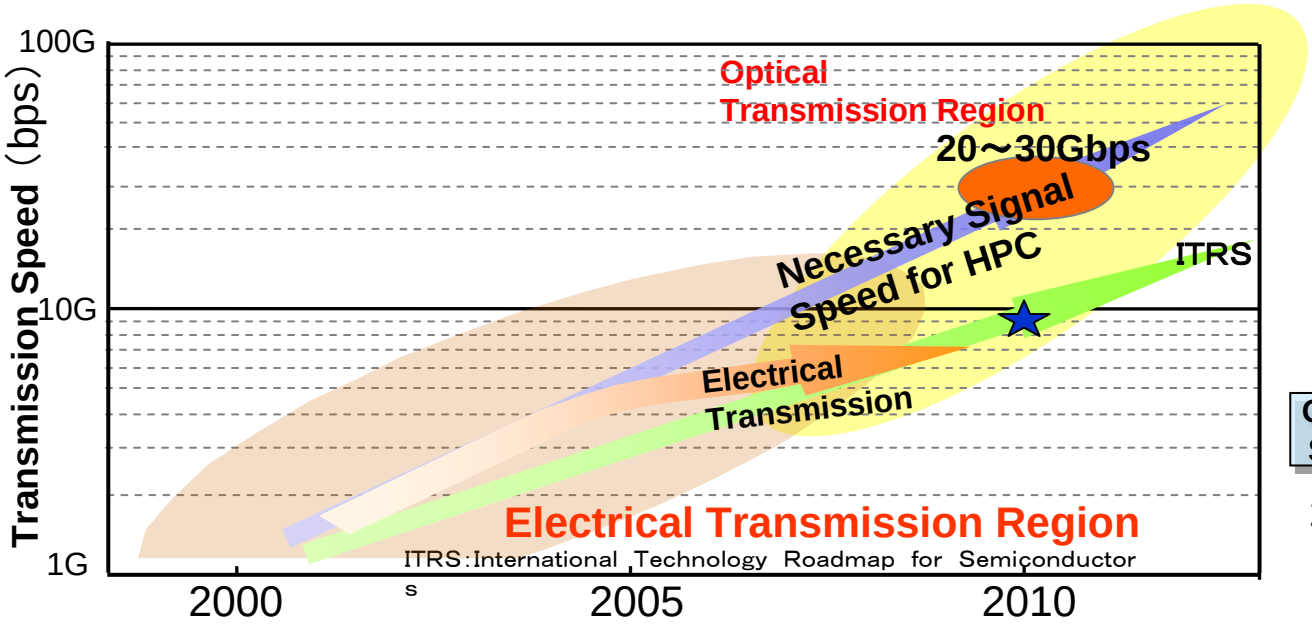
Electric Wiring

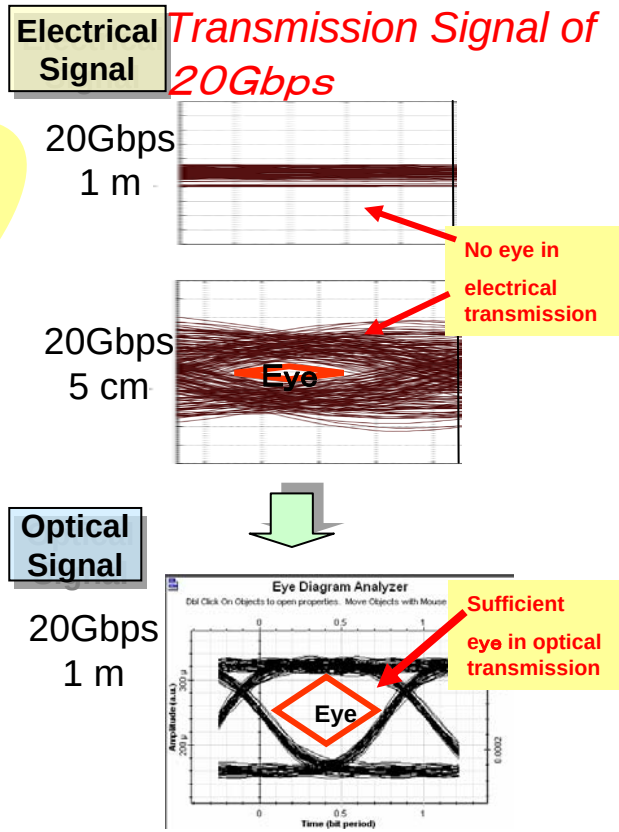
Optical Wiring



NEC

Signal Transmission（Chip to Chip）

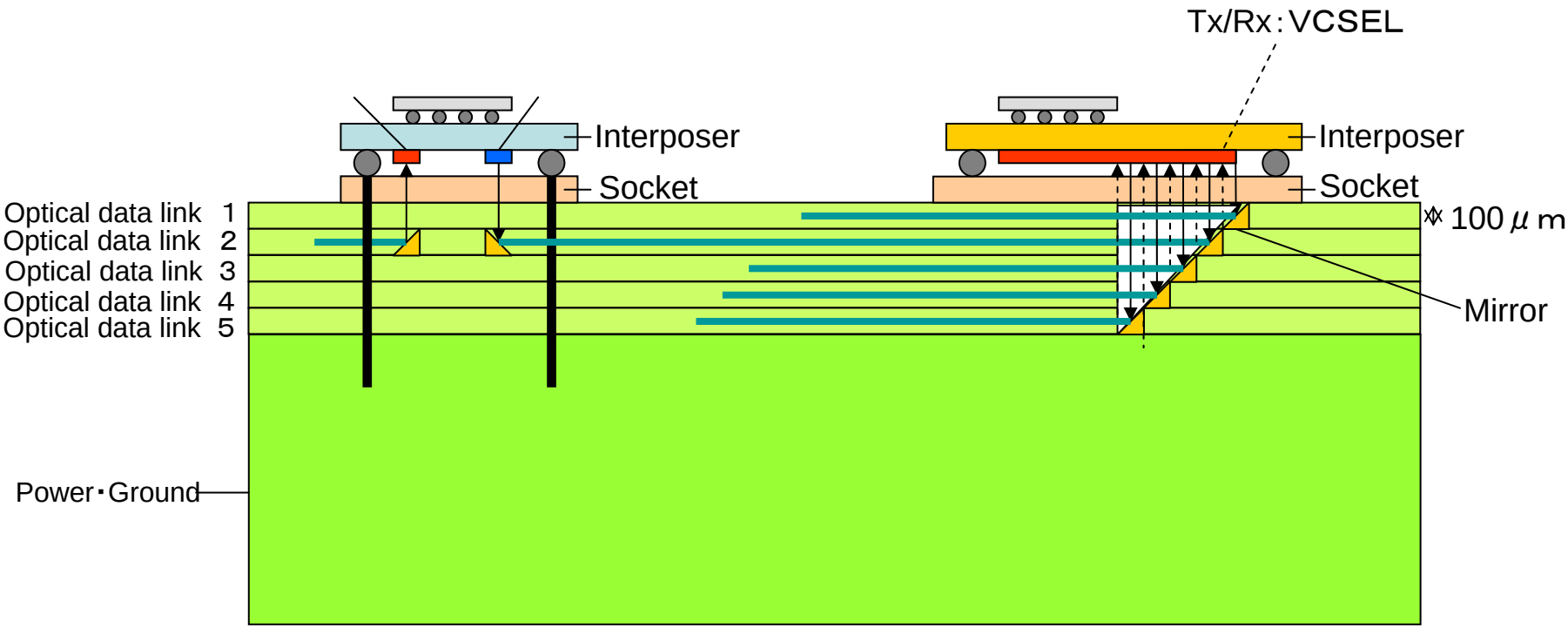




NEC

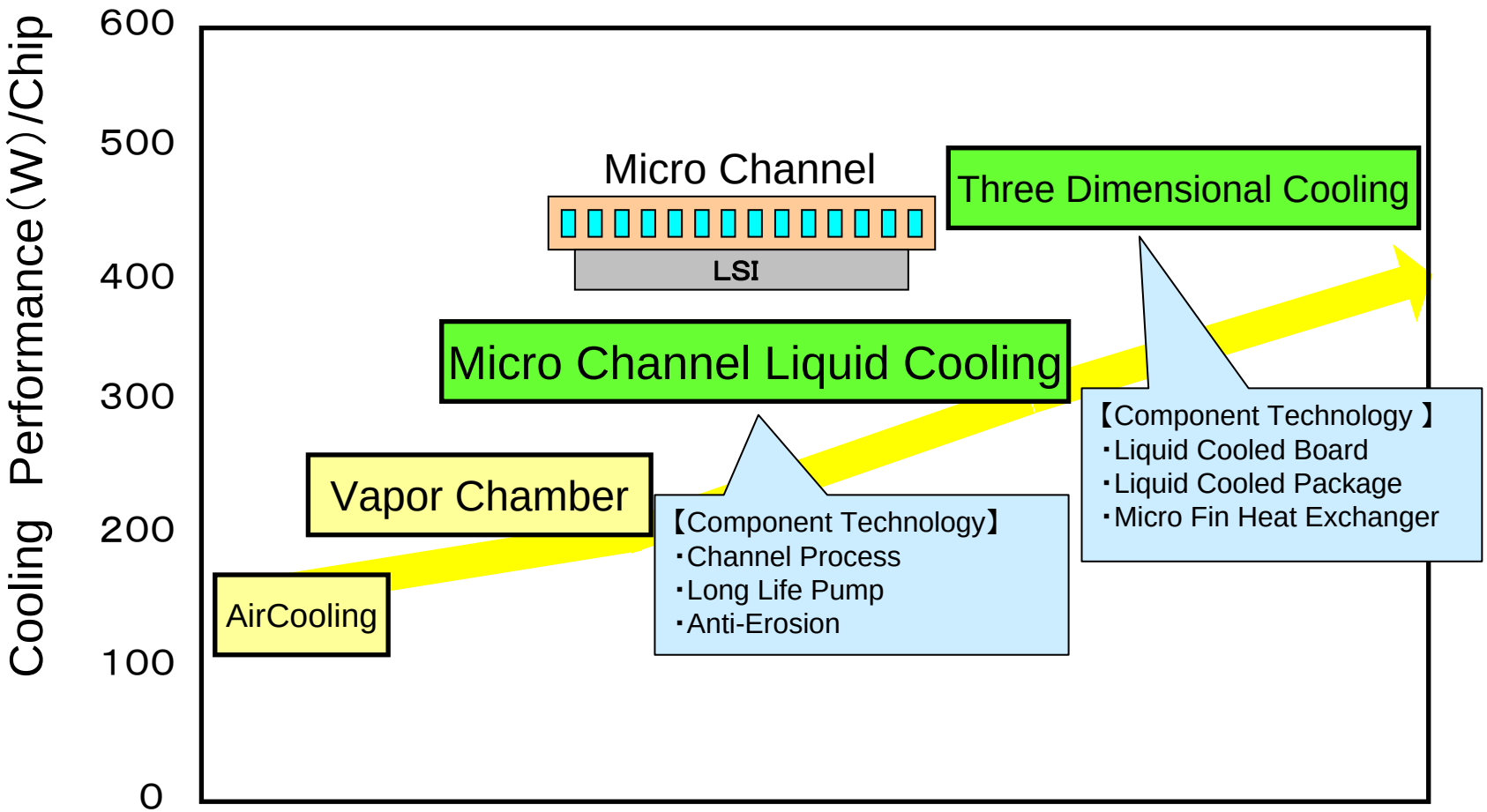
Optical Interconnection（Chip to Chip）

- **High Density Optical Interconnection by Multi-Layer Wave Guide**
- **Optical Cross Interconnection**



NEC

Cooling Technology



NEC

Future Technologies after Si

1.Single Flux Quantum Device（SFQ）

2.Quantam Computer

NEC

1.Single Flux Quantum Device（SFQ）

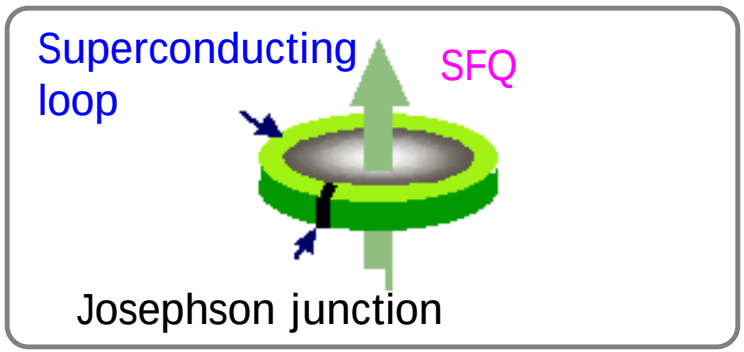
NEC

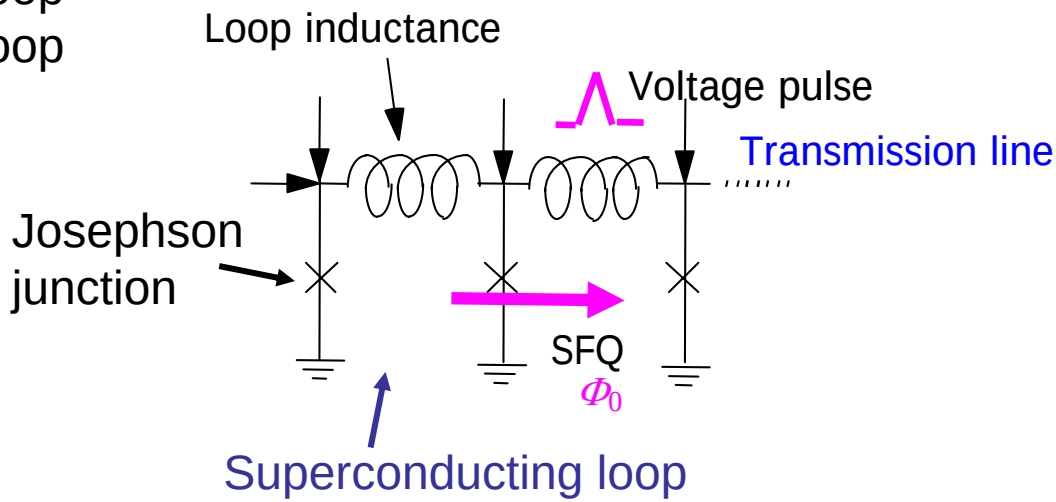
Nb-based Superconducting SFQ (Single Flux Quantum) circuits

- Unique device which can realize higher clock-speed LSIs than semiconductor devices
  - Ultra high speed and low power nature
    - cf. CMOS LSI: Big barrier against clock-speed higher than 10 GHz because of power and wiring problems
    - Compound semiconductors: LSI impossible because of large power consumption

Signal propagation at the speed of light in superconducting transmission lines

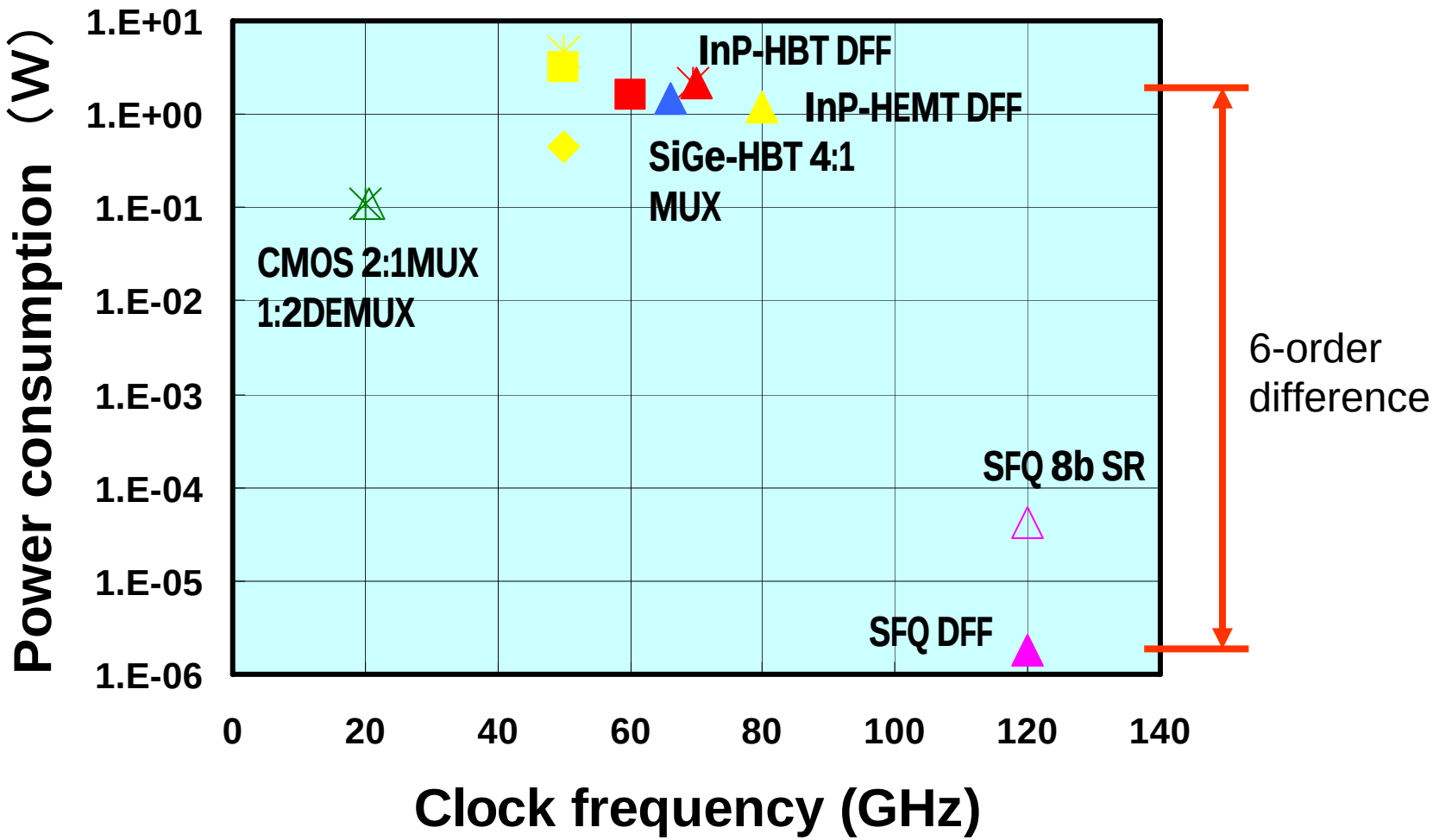
"1" : an SFQ in a superconducting loop
"0" : no SFQ in a superconducting loop





NEC

Comparison with Semiconductor and SFQ high-speed gates



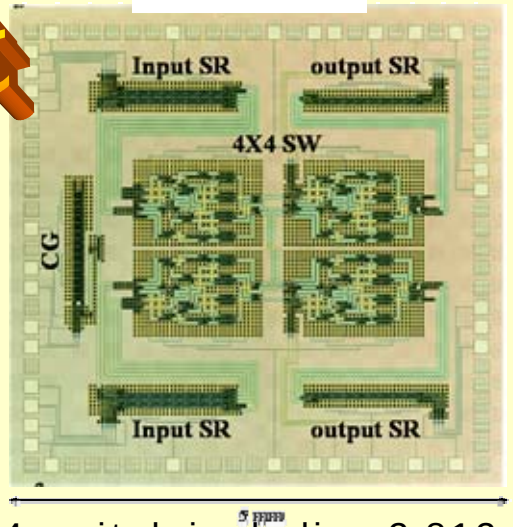
High-speed and large-scale integrated circuits can be realized by the SFQ technology

NEC

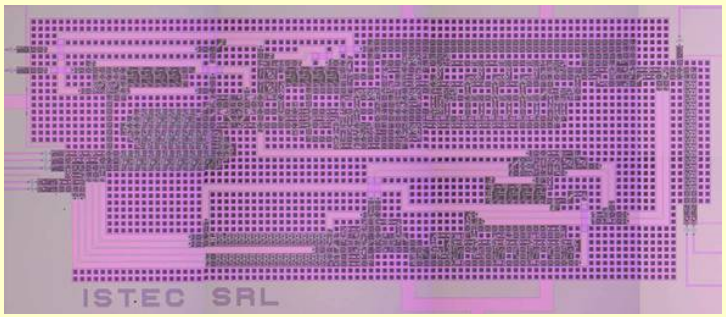
Examples for operated SFQ LSIs

Router

Fast



4x4 switch including 2,812 JJs operated up to 40 GHz.

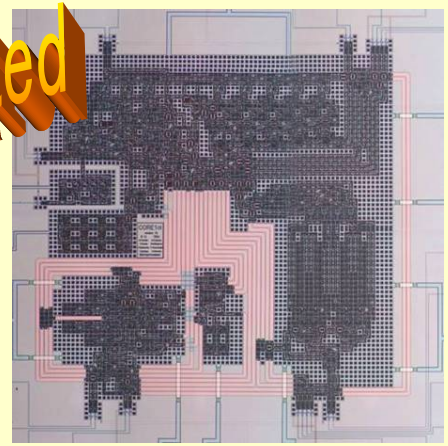


4x4 switch scheduler including 3,071 JJs operated up to 40 GHz.

by SRL

Microprocessor

Complicated

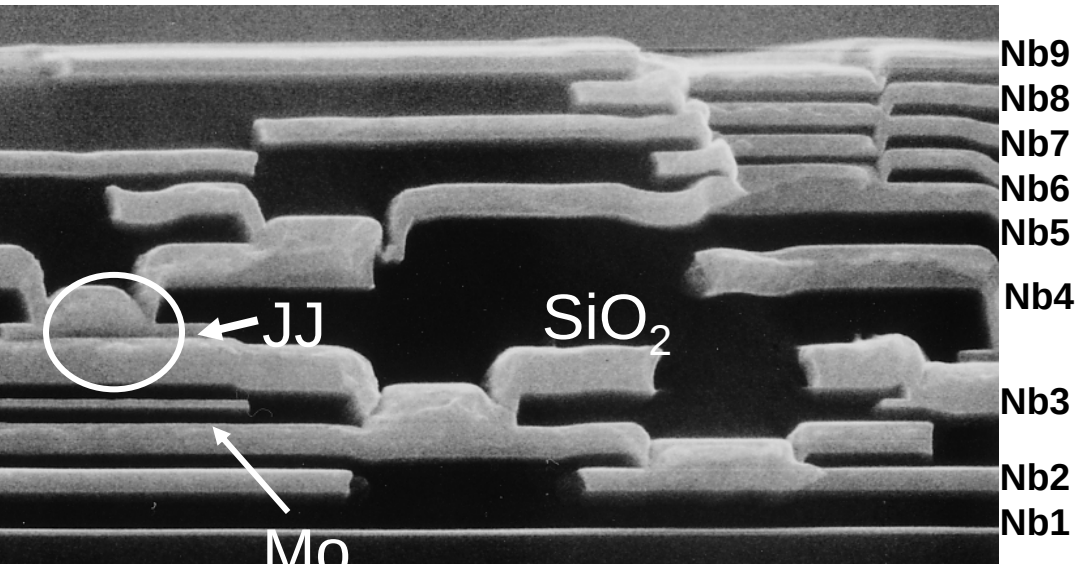


Microprocessor including 7,220 JJs fully operated up to 21 GHz.

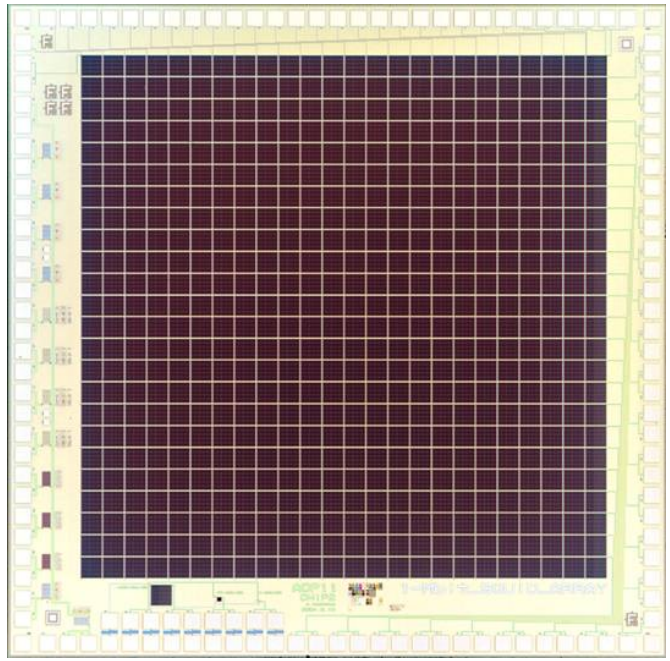
by Nagoya Univ. & Yokohama Nat'l Univ.

NEC

Toward larger-scale SFQ integrated circuits



Cross section view of a Nb nine-layer structure



1 million SQUID (2 million JJs) on a 8 mm square chip.

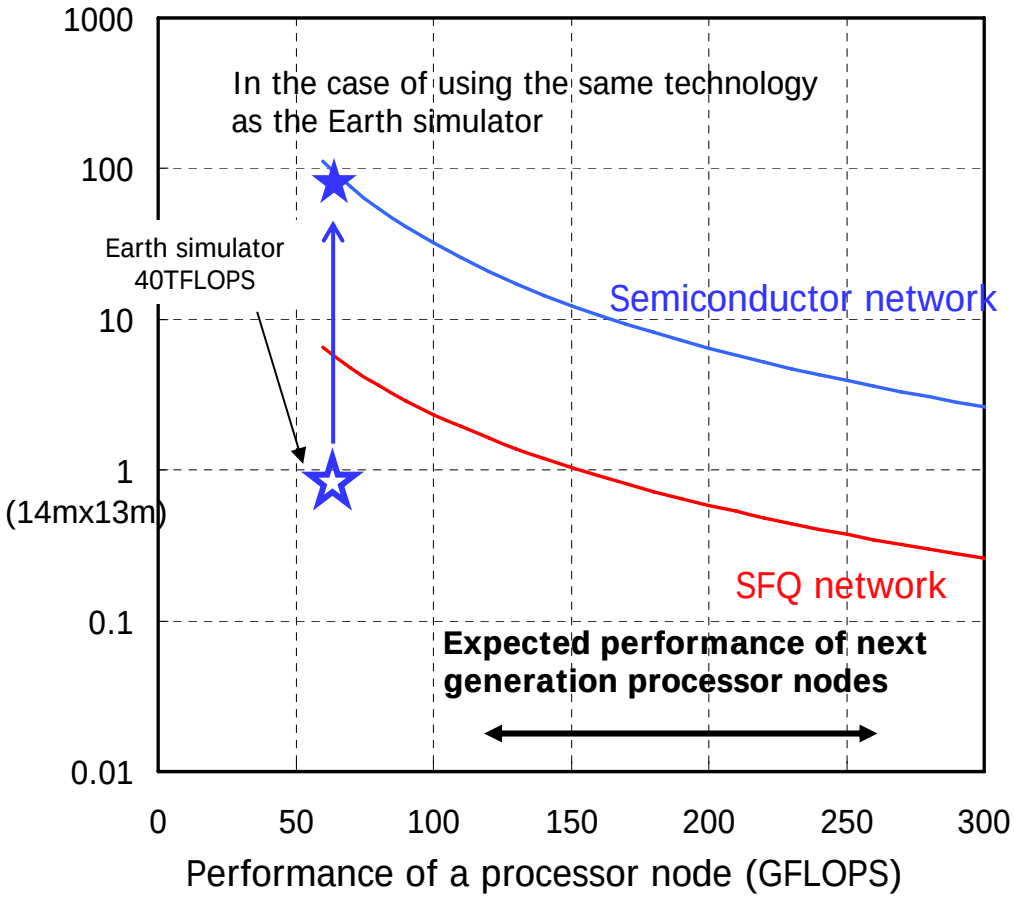
Developed new fabrication process

↓

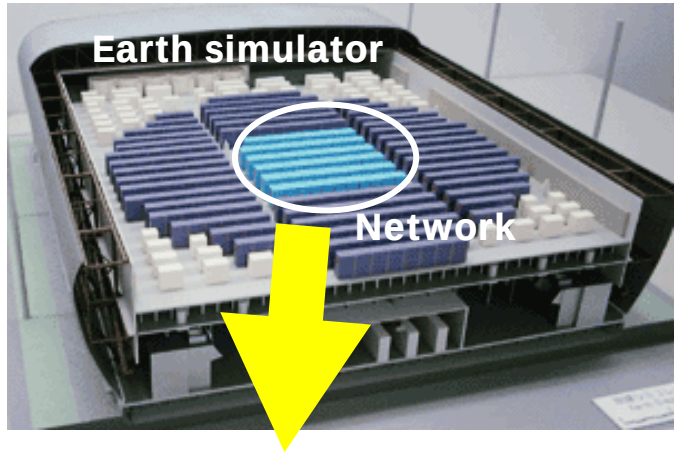
Larger scale and higher speed

NEC

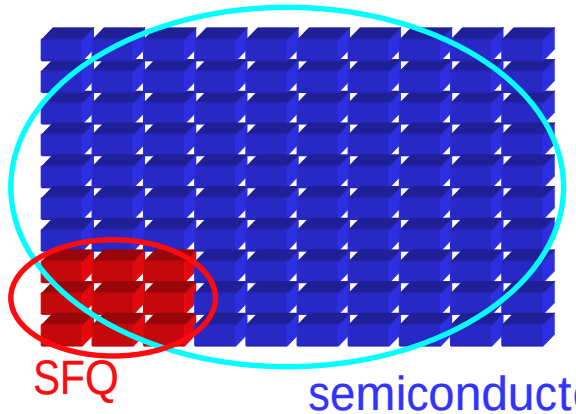
Estimation of a supercomputer network area reduction by using SFQ switches



Network area for a 400 TFLOPS supercomputer normalized by the Earth simulator network area



SFQ is the key technology for saving area



Reduce network area to 1/10 by the SFQ technology

2.Quantam Computer

NEC

Ultra-High Speed Computing

Quantum Computer

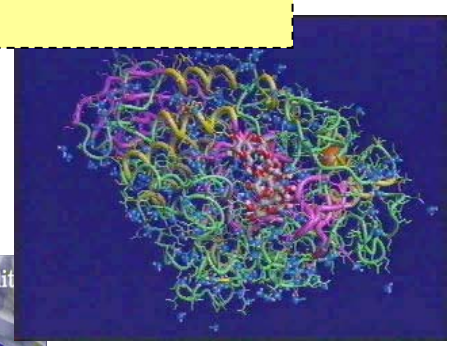
FLOPS = F (Calculation Speed)

1Peta-F
(1,000 Trillion OPS)
100 Tera-F
10 Tera-F
1 Tera-F
(1 Trillion OPS)
100 Giga-F
10 Giga-F
1 Giga-F
(1 Billion OPS)

NEC SX-6

Peta-Flops Computer

Earth Simulator (JAMSTEC)



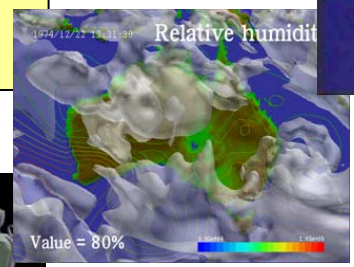
Protein analysis

NEC Parallel Computer Cenju-4

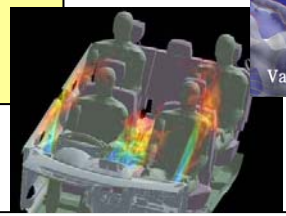
Super-computer

Server

PC



Atmospheric temperature



Flow of wind from air conditioner

Applicable Fields

Building analysis
LSI heat analysis

Wind flow analysis
Car collision analysis

Global climate

Bio

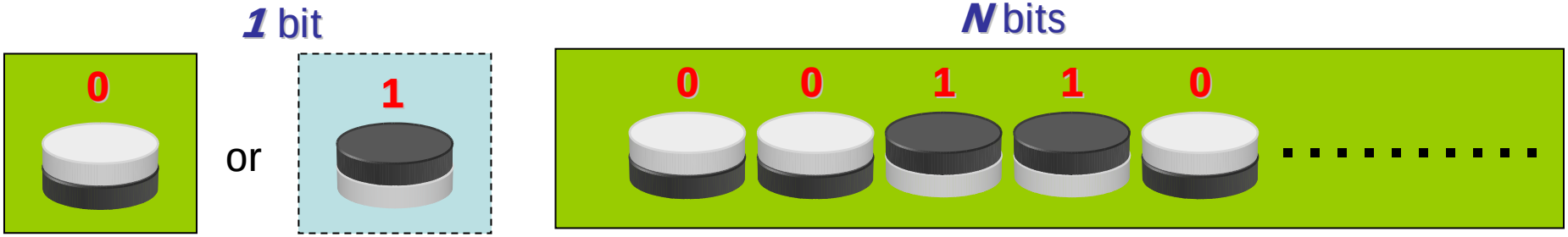
Representative Industries

Construction/Iron & Steel | Heavy Industries | Automobile | Climate/Environment | Medicine/Drug/Health | Farming/Food/Chemistry | Oil/Energy/Environment

※FLOPS: Number of calculations per second

Principle of qubit state

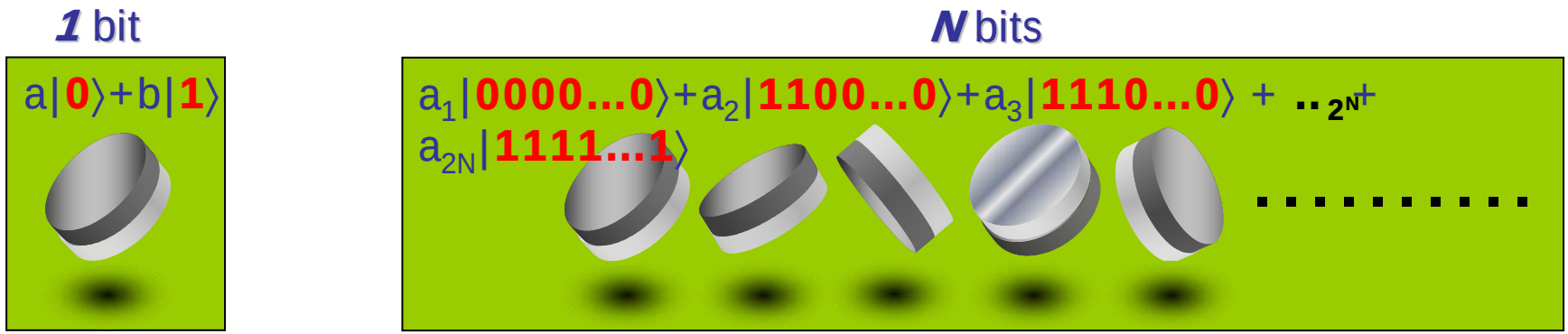
Usual bit information



One of “0” or “1”

One pair of 2^N combination

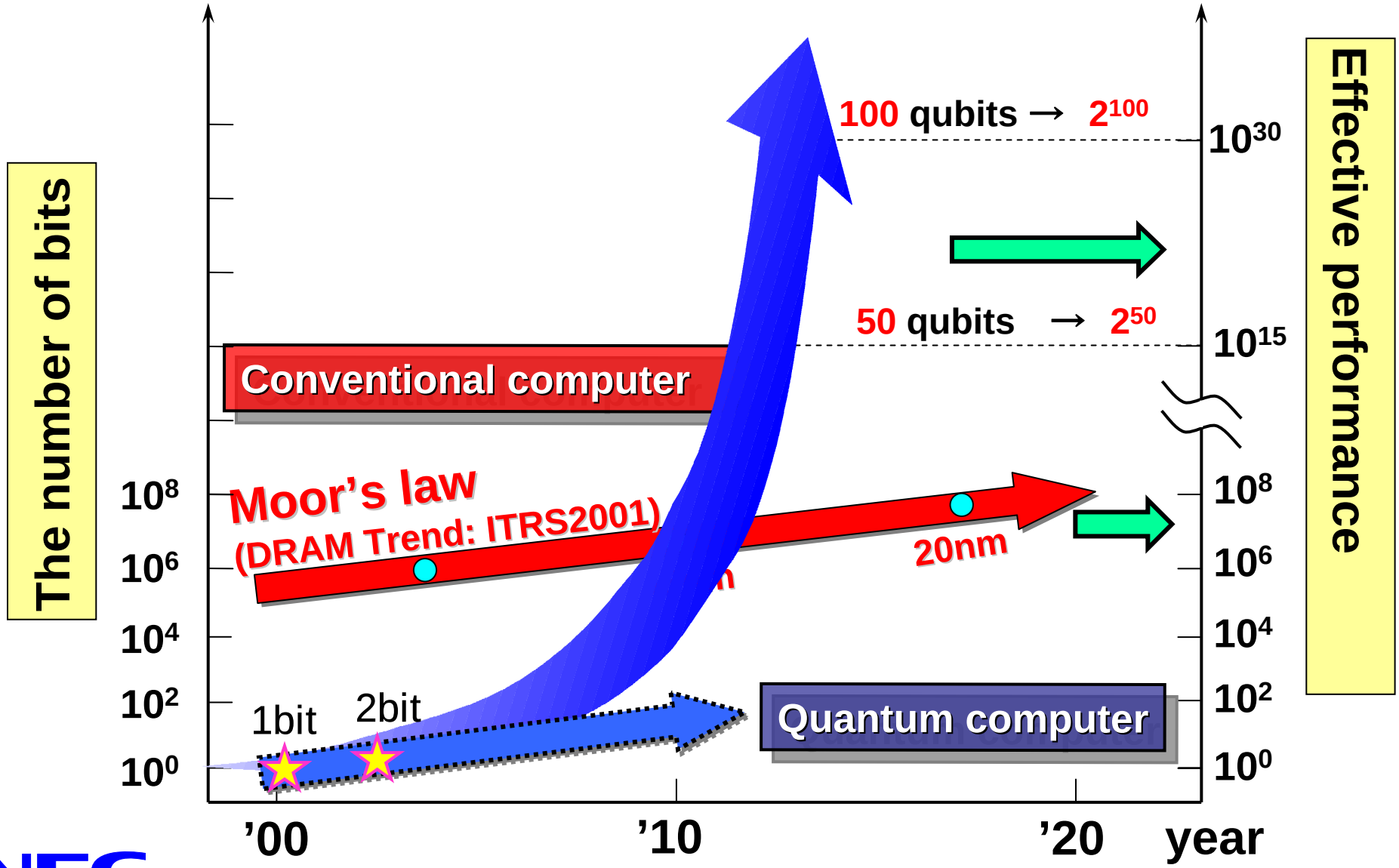
Quantum bit information



Combination of “0” and “1”

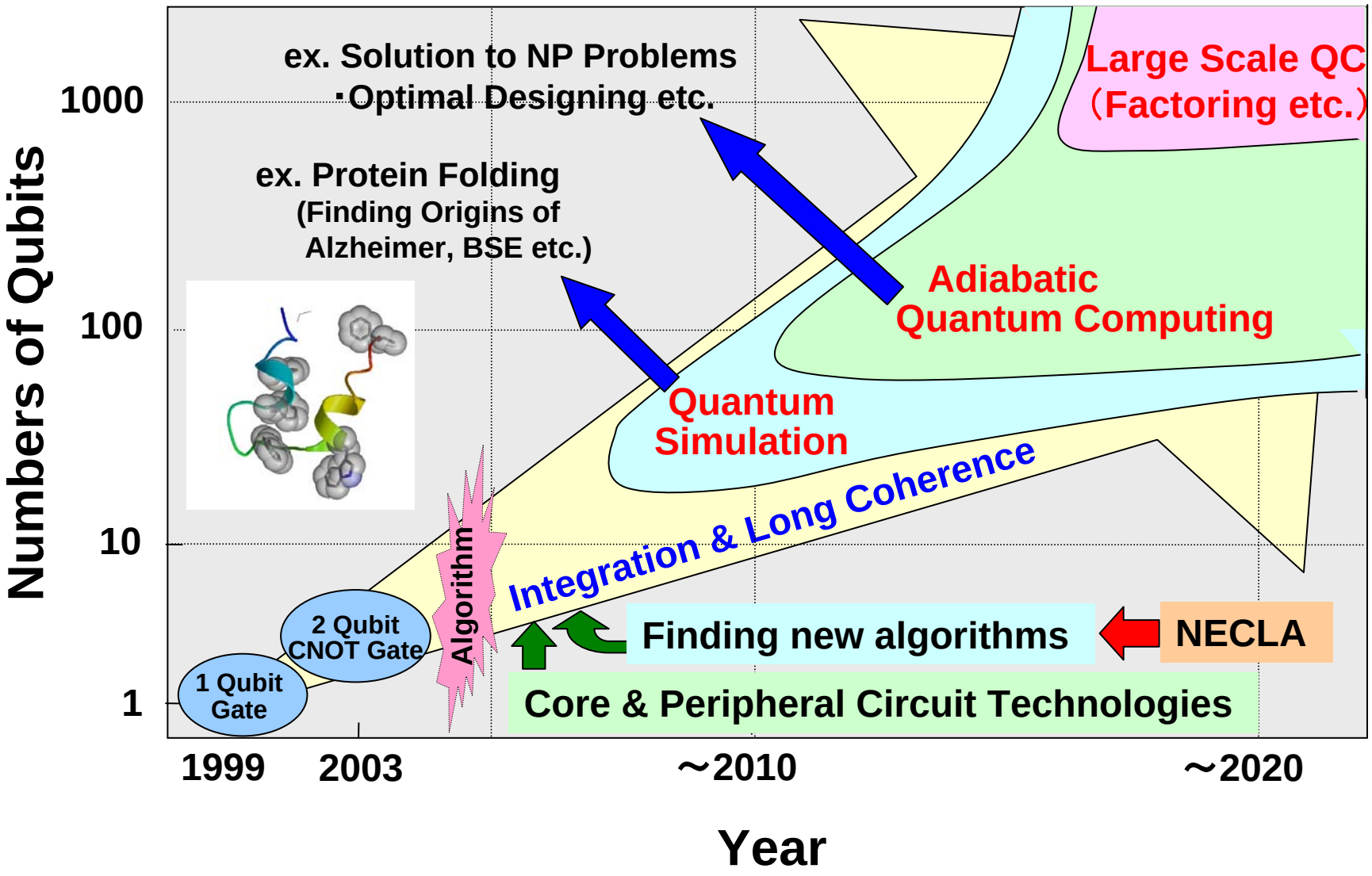
combination of 2^N states

Ultimate performance of quantum computing



NEC

Road Map of Quantum Computation



NEC

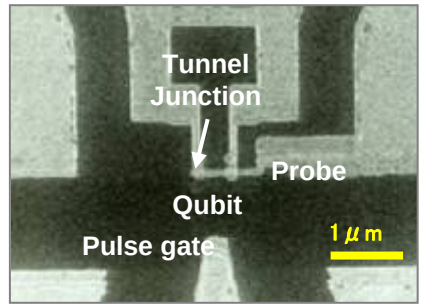
Solid State Qubits by NEC

Apr.1999 Coherent control of macroscopic quantum states in a single-Cooper-pair box

（Control of Superposition）

(Nature Vol.398, '99)

Magazine Cover →



Feb. 2003 Quantum oscillations in two coupled charge qubits

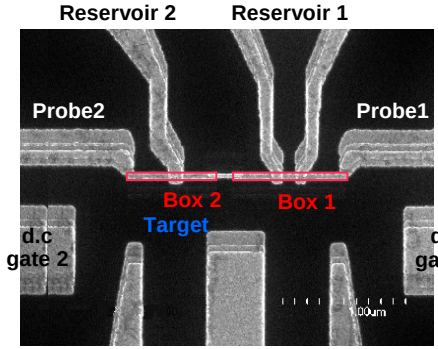
（Entanglement Creation）

(Nature Vol.421, '03)

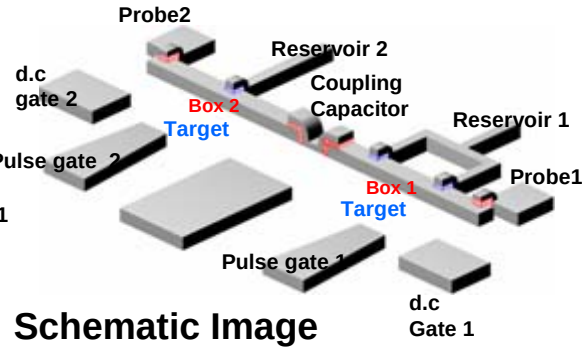
Oct. 2003 Demonstration of conditional gate operation using superconducting charge qubits （CNOT operation）

What Can Quantum Computer Do?

1. Problems that the modern computer can not solve, like factoring large numbers.
2. Simulation of complex quantum systems, like proteins, nano-materials, and others.
3. Applications to quantum communication.



Micrograph



Schematic Image

(Nature Vol.425, '03)

Conclusion

- We can see technologies for up to 45nm process.
- After 45nm,there are several technologies, but yet unseen.
- After Si, new technologies are emerging, but still experimental.

  It will take more than 10 years for actual use.

NEC

Finally,

Engineers usually take it pessimistic, because they always face technical barriers and difficulties, and must make risky challenges.
Looking back the past, however, most of technical barriers have been overcome, and what we dreamed in the past has been realized.

I have never imagined tera-flops nor peta-flops computing when I started the development of the first giga-flops computer.
The tera-flops was a dream,
but the tera-flops computers are already in use, and the peta-flops will surely come in 2010.

A dream will be in reality only when continuous efforts to realize it have been made.

NEC