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Turbo Equalization as a Postprocessor for Partial-Response Channels.

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Introduction
Post-Viterbi processors are used for detection of partial-response channels coded with weak parity codes, whereas turbo equalization is usually used for detection and decoding of strong low-density parity check (LDPC) codes. This digest discusses the use of turbo equalization for joint detection and decoding of parity codes that would be used in postprocessing systems. The proposed system has complexity significantly lower than conventional LDPC-turbo equalization systems, and has excellent performance vis-a-vis postprocessing systems. The flexibility of the proposed system is demonstrated by considering an unequal error protection (UEP) code which preferentially places Viterbi algorithm error events within Reed-Solomon symbol boundaries to decrease the sector error rate. For longitudinal recording systems, single-parity checks on a sequence of adjacent bits, or on an interleave of those bits [1] are effective for detecting and correcting dominant odd-weight bit error patterns. For perpendicular magnetic recording channels, parity-check codes for correcting dominant even-weight bit-error patterns have been proposed [2]. We show parity codes to be effective on perpendicular recording systems when decoded by turbo equalization, even though these codes are not matched to specific detector error patterns. An idealized AWGN partial-response channel with impulse response (4,6,4,2) for perpendicular magnetic recording is considered. Turbo equalization is performed at the receiver, and one iteration of turbo equalization consists of one use of the BCJR algorithm for channel detection, followed by one use of the message-passing algorithm for decoding the parity code. Single-Parity Check Codes The performance of a rate R=(n-1)/n, interleaved single parity check code, with check matrix H_0 and block length N is considered. Let M=N/n be the number of parity checks. The parity check matrix for this code can be represented by a concatenation of identity matrices I_M, H_0 = [I_M I_M ... I_M]. A rate R=50/51 code was used on the idealized channel and decoded for one to three turbo iterations. After three iterations, a coding gain of 1.3 dB and 1.6 dB at probability of bit error of 10^{-4} and 10^{-5}, respectively, was observed. For a rate R=64/65 code, the corresponding gains were 1.2 dB and 1.5 dB. In all simulations N of approximately 4000 is used. Relative to strong LDPC-coded turbo equalization systems, the message-passing decoder complexity in the proposed system is substantially lower. The parity portion of the message-passing graph has only N messages, and no computation is required at the bit node, which has degree one. Most of the performance benefit is obtained after two iterations, and a third iteration gives only a marginal improvement in the BER. UEP Parity Codes The above code can be modified to improve the performance of a system which uses an outer Reed-Solomon code, constructed over GF(2^q). The turbo equalizer finishes on a half-iteration with the Viterbi algorithm, and its hard output passed to the Reed-Solomon decoder. If a Viterbi error event spans two (or more) Reed-Solomon code symbols, then both (or all) symbols must be corrected. The performance of the concatenated system is improved by using a UEP parity code [3] where bits near the Reed-Solomon codeword boundaries are protected strongly, and the remaining bits are protected by a single parity check. The goal is to increase the probability that error events fall entirely within a single Reed-Solomon codeword symbol. The parity check matrix for the proposed UEP code, H_1, is constructed in the following way. Columns i=1,2,..N for which i mod q = 0 have column weight r, correspond to strongly protected bits, and the remaining columns have weight one, corresponding to weakly protected bits. The row weight of H_1 is constant, N(q-1+r)/(Mq). The construction of H_1 begins with H_0, then adds bits pseudo-randomly to the strong columns such that the row and column weight constraints are observed. The sector error rate of such a system is computed using multinomial analysis, where the probability of sector failure is found from the distribution of independent symbol failures of different lengths. In the analysis, a (430,410,10) Reed-Solomon code is used to encode a single sector. Symbol error statistics are estimated from simulations. A R=49/50, r=2 UEP code is used, and compared with a R=49/50 SPC code. As can be seen from the estimated sector error rate performance in Fig. 1, significant coding gains are obtained by using a UEP code.

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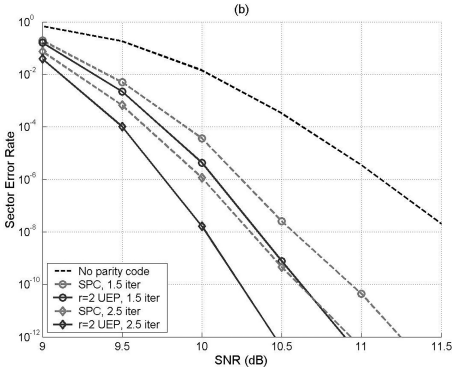

SER of R=49/50 single parity check (SPC) and unequal error protection (UEP) codes, with (430,410,10) RS code.