Turbo Equalization With Single-Parity Check Codes and Unequal Error Protection Codes

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The performance of turbo equalization with interleaved single-parity check codes on partial-response channels is evaluated. Single-parity check codes are weak codes, but are shown to have modest performance gain. The proposed system achieves gains of 3.5, 3.4, 2.7, and 2.4 dB with code rates of 19/20, 24/25, 49/50, and 63/64, respectively, at a BER of 10^{-5}. The complexity of the proposed decoder is significantly lower than that of turbo equalization using standard low-density parity-check codes. These single-parity check codes are modified to be unequal error protection codes, designed to decrease the probability that Viterbi error events span Reed–Solomon symbol boundaries, resulting in a decrease of the sector error rate. Once such code gains an additional 0.1 dB over a single-parity check code of the same code rate of 24/25.

***Index Terms*—Intersymbol-interference channels, partial-response channels, post-processing, turbo equalization.**

I. Introduction

TURBO equalization has excellent performance gains on partial-response channels when using strong outer codes, such as low-density parity-check (LDPC) or turbo codes, or the combination of an outer convolutional code and precoder [1]–[3]. For an LDPC code with a sparse parity-check matrix with constant column weight j, Gallager showed that asymptotically good distance properties are obtained for $j \geq 3$. Nonetheless, good performance on magnetic recording channels can be obtained using LDPC codes with column weight $j = 2$ [1]. However, turbo equalization requires a large number of iterations with complex soft-output decoding algorithms. Further, many proposals have code rates which are comparatively low, e.g., 8/9.

Turbo equalization with single-parity check codes, which are $j = 1$ LDPC codes, is considered in Section II. Such codes are weak, but have high rates and obtain modest coding gain. Due to the simple nature of the codes, the complexity of the proposed decoder is considerably lower than for $j \geq 2$ LDPC-coded systems. We note that previous approaches have used single-parity check codes on magnetic recording channels, in a parallel concatenation [2] or in a serial concatenation with a precoder [3]. These constructions result in strong codes with parity-check matrices with many columns of weight greater than 1, distinct from the work here.

Simple, high-rate parity-check codes have been used as part of a post-Viterbi processor. These codes are designed to detect specific error events, for example see [9] for longitudinal channels and [4] for perpendicular channels. In [5], a postprocessor using interleaved single-parity check codes was proposed. As with our work, that system does not require knowledge of specific error events.

Reed-Solomon (RS) codes are effective for correcting error bursts produced by a Viterbi error event, as a burst occurring entirely inside one symbol causes a single RS symbol error. However, any error event of length greater than one can span multiple symbols, requiring multiple corrections by the RS code.

In Section III, we mitigate this problem of error events which span multiple RS symbols by modifying the parity codes to create unequal error protection codes [6]. Bits near the RS symbol boundary are strongly protected from errors, whereas bits far from the boundary receive standard protection. This reduces the overall sector error rate when RS codes are used.

To evaluate the proposed system, the following idealized, white-noise magnetic recording channel is used. Let x_j be bits of an LDPC codeword with rate R, parity-check matrix H and block length N, with $j = 0, \ldots, N-1$. The intersymbol-interference channel has impulse response $h(D) = h_0 + h_1 D + \cdots + h_\nu D^\nu$. The receiver observes $y_j = \sum_{i=0}^{\nu} h_i x_{j-i} + n_j$, where n_j is additive white Gaussian noise (AWGN) with known variance σ^2. The signal-to-noise ratio (SNR) is E_s/RN_0, where E_s is the average power in the noiseless channel output and $N_0 = 2\sigma^2$.

Turbo equalization with an LDPC code is performed at the detector, where one turbo iteration consists of one use of the channel detector, followed by one use of the decoder. The channel detector is the Bahl–Cocke–Jelinek–Raviv (BCJR) algorithm. The decoder is the sum-product algorithm operating for one local iteration. The iterative turbo decoder may terminate with either the sum-product algorithm or the channel detector. When the sum-product algorithm is used last, hard decisions are made on the sum of the outputs of the BCJR and sum-product algorithms; this case is indicated as $1, 2, 3, \ldots$, turbo iterations. When the channel detector is used last, the Viterbi algorithm is used instead of the BCJR algorithm, where *a priori* information provided by the sum-product algorithm is incorporated into the transition metrics; this case is indicated as $1.5, 2.5, \ldots$, turbo iterations.

II. Single-Parity Check Codes

In this section, the error rate performance of an interleaved single-parity check code is evaluated. The code has M-by-N parity-check matrix H_0, and rate $R = (n-1)/n$, with integer $n \geq 2$, so $M = N/n$. The parity-check matrix for this code can

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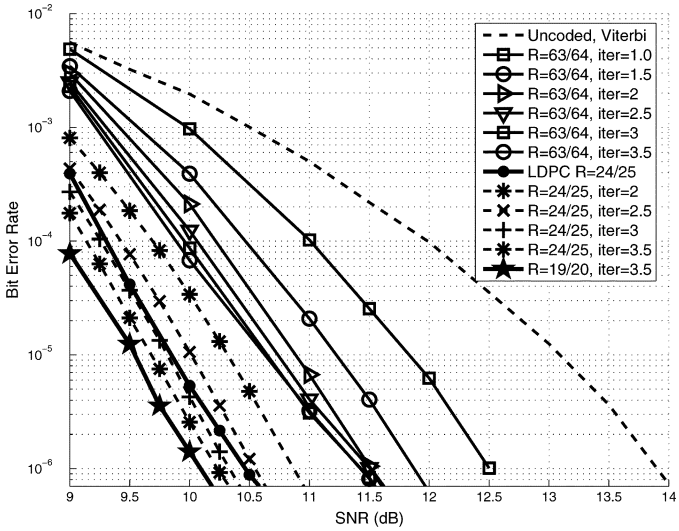

Fig. 1. BER of interleaved single-parity check codes for various rates; a column weight 2 LDPC code, decoded for 3.5 iterations, is shown for reference.

be represented by a pseudo-random column permutation of the concatenation of M-by-M identity matrices I_M, with $H_0 = [I_M \; I_M \; \cdots \; I_M]\Pi_N$, where Π_N is a N-by-N permutation matrix.

The channel response $h(D) = 4+6D+4D^2+2D^3$ was suggested as a partial-response target for perpendicular recording with a normalized recording density of 1.4 [7]. In our simulations, we use this polynomial for an idealized, white-noise channel. Codes with a block length of $N \approx 4000$ are used. Fig. 1 shows the BER performance of these single-parity check codes. Codes of rates $R = 19/20, 24/25, 49/50$ and $63/64$ achieve gains of 3.5, 3.4, 2.7(not shown), and 2.4 dB after 3.5 iterations at a BER of 10^{-5}. Also shown is a rate $24/25$ LDPC code with column weight $j = 2$, after 3.5 iterations. For the parameters shown, this code has inferior BER performance; however, as the number of iterations increase, the LDPC code performs better than the single-parity check codes, but at the expense of greater decoding complexity.

The complexity of the sum-product decoding algorithm is proportional to the number of ones in the parity-check matrix, and thus decoding the single-parity check code has half the complexity of decoding LDPC codes with $j = 2$. Furthermore, no computation is required at the bit node, as *a priori* information is passed directly from the check node to the BCJR algorithm. In the absence of intersymbol-interference, the joint factor graph representing the code and channel is cycle-free and decoding would converge in one iteration. With intersymbol interference, the rate $63/64$ code converges in two iterations at high SNR.

III. Unequal Error Protection Codes

In this section, the performance of a system with an outer RS code is improved by using an unequal error protection code designed to decrease the probability that an error event spans two RS code symbols. A (n, k, t) RS code, constructed over $\mathrm{GF}(2^q)$, can correct up to t symbol errors from a block of n symbols, of which k are information symbols. Adjacent bits x_j are placed in groups of q to form symbols from $\mathrm{GF}(2^q)$.

For the proposed unequal error protection code, bits x_j for which $j \bmod q = q-1$ are at the RS symbol boundary and are protected strongly, and the remaining bits are protected weakly. The M-by-N parity-check matrix for this code is H_1. Columns of H_1 for which $j \bmod q = q-1$ have weight r, and the remaining columns have weight one. The row weight of H_1 is constant, $(N(q-1+r))/(Mq)$. The construction of H_1 begins with H_0, then adds bits pseudorandomly to the strong columns such that the row and column weight constraints are observed. The unequal error protection code has the same rate as the original single-parity check code. This code is an irregular LDPC code; irregular LDPC codes have been recognized as unequal error protection codes [8]. Under sum-product decoding, the strong bits combine messages from r check nodes to increase the message reliability, whereas the weak bits use a single check only. During turbo equalization, strong *a priori* information passed to the channel detector decreases the probability that an error event will cross a symbol boundary.

We consider turbo equalization which finishes on a half-iteration using the Viterbi algorithm, so that we may characterize the effects of the unequal error protection code on the error event distribution at the output of the turbo equalizer. Unequal decoder-to-detector reliability information leads to an unequal error event distribution, but error events which begin in positions $j \bmod q$ have uniform characteristics, ignoring end effects. In particular, p_l^k is the joint probability an error event of length l bits begins in position $k = j \bmod q$. Let $P(k, s)$ be the joint probability that an error event which begins in position k will span s RS symbols. Then

$$P(k,s) = \sum_{z=(s-1)q-k+1, 1\le z\le N}^{sq-k} p_z^k. \tag{1}$$

The marginal symbol error distribution is $P_s = \sum_k P(k, s)$.

Multinomial analysis can be used to estimate sector error rates when an outer RS code is used [9]. The probability of sector failure P_W, which includes both RS decoder errors and decoder failures, can be computed from the distribution of independent symbol failures of length $s_i, i = 1, 2, \ldots,$

$$P_W \ge 1 - \sum_{s_0} \cdots \sum_{s_m} \frac{n!}{s_0! \cdots s_m!} P_0^{s_0} \cdots P_m^{s_m} \tag{2}$$

where P_0 and s_0 denote the probability of no error in a single symbol, and the number of such symbols, respectively. The sum is taken over $\sum_i i s_i \le t$ and $\sum_{i=0}^m s_i = n$. The interleaved nature of the parity-check matrix introduces correlation between error events assumed to be independent; thus (2) represents a lower bound on the sector error rate. This bound was found to be good for low SNR, and diverged for increasing SNR.

In the following numerical results, we assume that a shorted RS code over $\mathrm{GF}(2^{10})$ is used as an outer code. The unequal error protection codes considered have strong column weight $r = 2$. For the SNRs and code lengths considered, it was found that using $r \ge 3$ did not improve performance.

For Viterbi detection of the channel $h(D) = 4+6D+4D^2+2D^3$, the dominant error events $\pm(+-)$, $\pm(+-+)$ and $\pm(+-0+-)$, with lengths $l = 2, 3, 5$ respectively, are considered. A

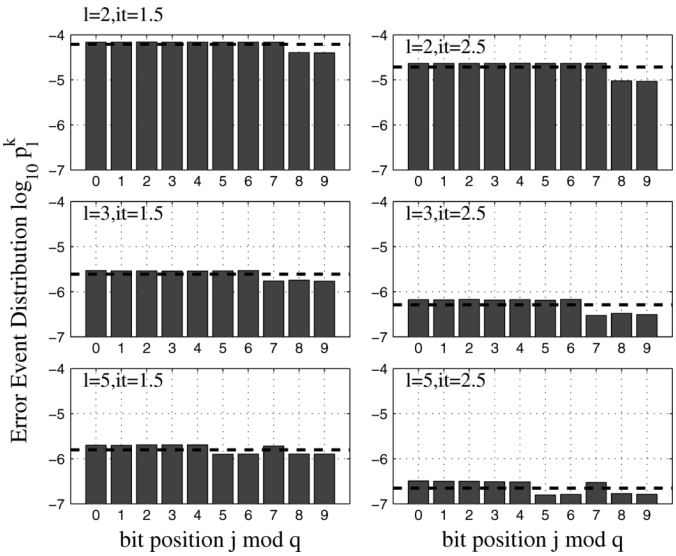

Fig. 2. For the unequal error protection code, error event distribution p_l^k versus beginning bit position $k = j \bmod q$, for event lengths $l = 2, 3, 5$, after 1.5 and 2.5 turbo iterations, at an SNR of 9 dB. Dashed lines show the error event distribution for the single-parity check code.

rate $24/25$, $q = 10$ unequal error protection code was used, and error statistics were collected at an SNR of 9 dB. The resulting error event distribution p_l^k is shown in Fig. 2, for error events of lengths $l = 2, 3, 5$ and for 1.5 and 2.5 iterations. Dashed lines indicate the error event distribution when the single-parity check code is used. As can be seen, the unequal error protection code is effective at reducing the probability that error events do not occur in positions for which $j \bmod q = q - 1$, that is, the error events which cross the RS symbol boundary. Note that at length $l = 5$, the dominant error event is $\pm(+-0+-)$, and the code does not reduce the probability that an error event begins in position 7, when the 0 element is in the strong bit position.

Fig. 3(a) shows sector error rates from a simulation comparing a single-parity check code and an unequal error protection code, both of rate $24/25$, assuming that an outer RS code with $t = 3$ is used. At a sector error rate of 4×10^{-4}, the single-parity check code gives 1.8 and 2.2 dB of gain after 1.5 and 2.5 iterations, respectively. The unequal error protection code gives an additional 0.1 dB of gain, with no rate penalty, for both cases. Also shown is the rate $24/25$, $j = 2$ LDPC code, which has inferior performance for a small number of iterations.

Symbol error statistics were collected and used to compute a lower bound on the sector error rate using (2) assuming a $t = 10$ RS code, which is shown in Fig. 3(b). Although Fig. 3(b) represents a lower bound, the performance gain seen in the simulations is also observed in this analysis.

The complexity increase in turbo equalization due the unequal error protection code is slight: the strong bit nodes, which represent a fraction $1/q$ of the nodes, require $r - 1$ additions. The number of ones in the parity-check matrix increases by a factor of $(r - 1)/q$.

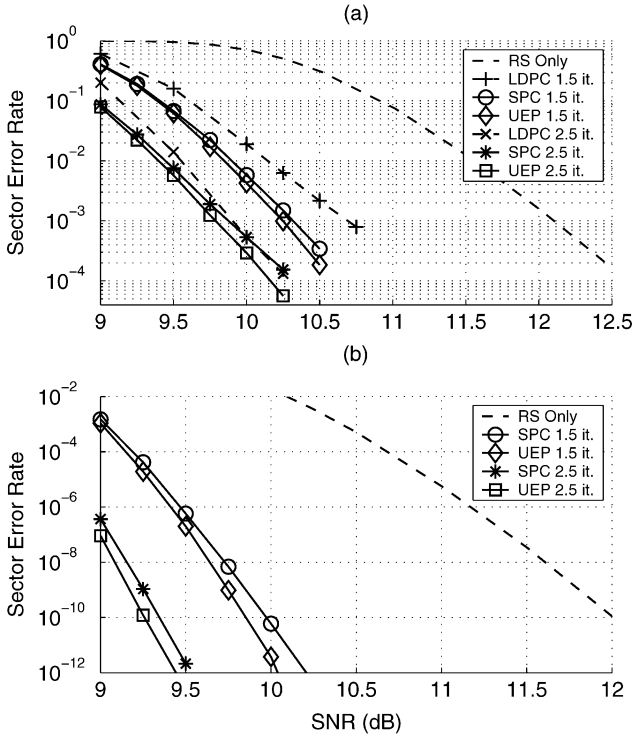

Fig. 3 (a) SER simulation of single-parity check (SPC) codes, $r = 2$ unequal error protection (UEP) codes, and $j = 2$ LDPC code; assuming a $t = 3$ RS code. (b) SER analysis for SPC and UEP codes, assuming a $t = 10$ RS code.

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